

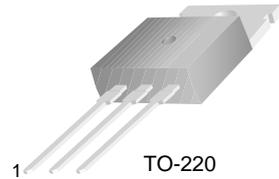


September 2011

KSC2073 NPN Epitaxial Silicon Transistor

Features

- TV Vertical Deflection Output
- Complement to KSA940
- Collector-Base Voltage : $V_{CBO} = 150V$



TO-220
1.Base 2.Collector 3.Emmitter

Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	150	V
V_{CEO}	Collector-Emitter Voltage	150	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	1.5	A
P_C	Collector Dissipation ($T_C = 25^\circ C$)	25	W
T_J	Junction Temperature	150	$^\circ C$
T_{STG}	Storage Temperature	- 55 to 150	$^\circ C$

Electrical Characteristics $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = 500\mu A, I_E = 0$	150			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = 10mA, I_B = 0$	150			V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = 500\mu A, I_C = 0$	5			V
I_{CBO}	Collector Cut-off Current	$V_{CB} = 120V, I_E = 0$			10	μA
h_{FE}	DC Current Gain	$V_{CE} = 10V, I_C = 0.5A$	40	75	140	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 500mA, I_B = 50mA$			1	V
f_T	Current Gain Bandwidth Product	$V_{CE} = 10V, I_C = 0.5A$		4		MHz
C_{ob}	Output Capacitance	$V_{CB} = 10V, I_E = 0, f = 1MHz$		50		pF

h_{FE} Classification

Classification	H1	H2
h_{FE}	40 ~ 80	60 ~ 125

Typical Performance Characteristics

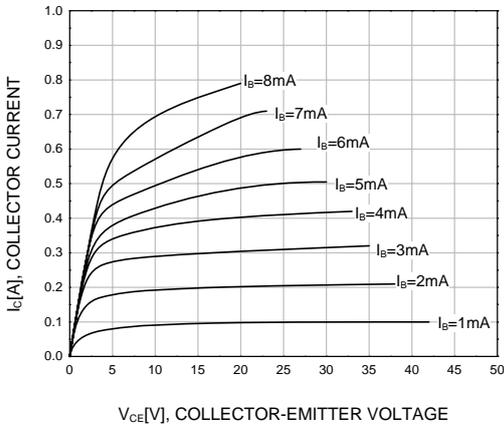


Figure 1. Static Characteristic

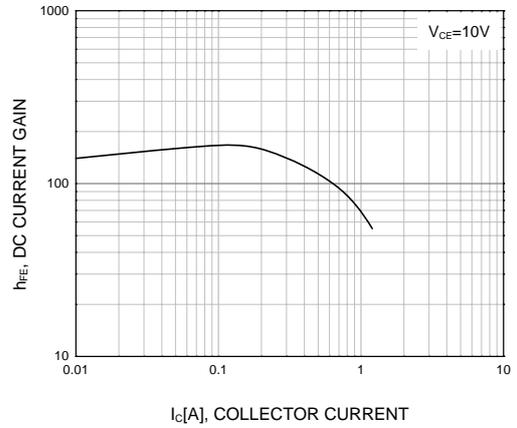
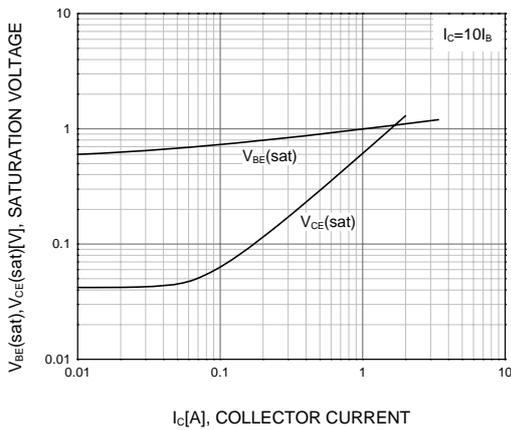


Figure 2. DC current Gain



**Figure 3. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage**

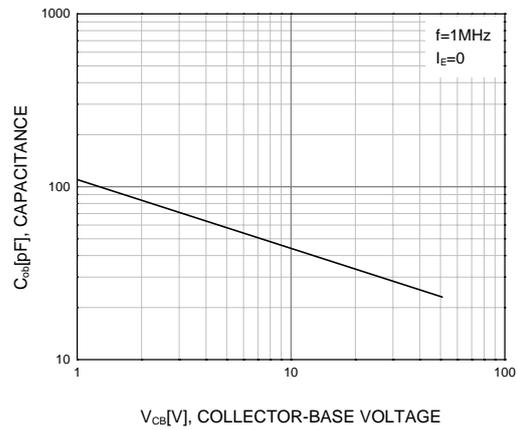


Figure 4. Collector-Emitter On Voltage

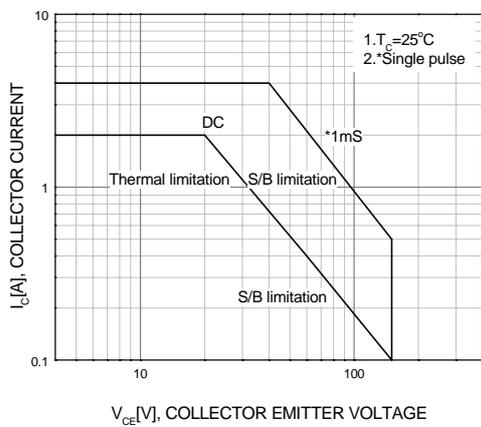


Figure 5. Safe Operating Area

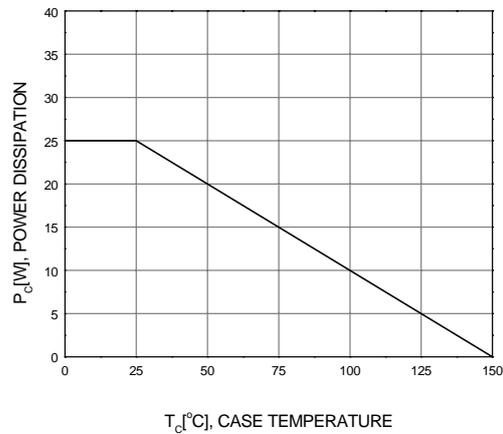
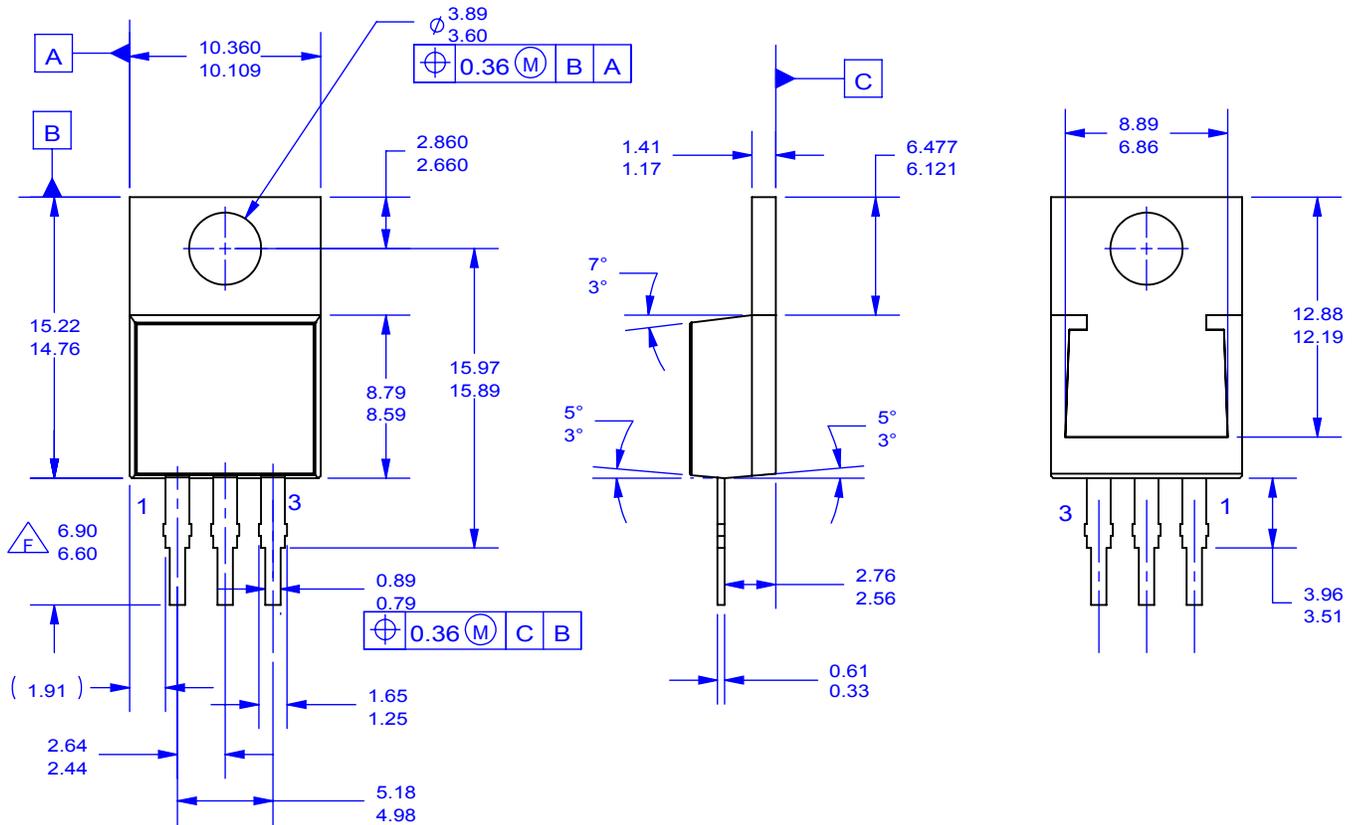
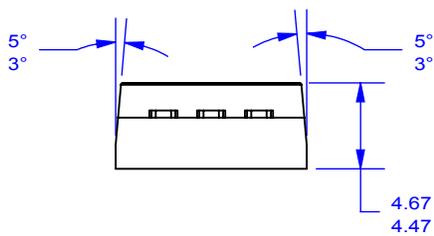


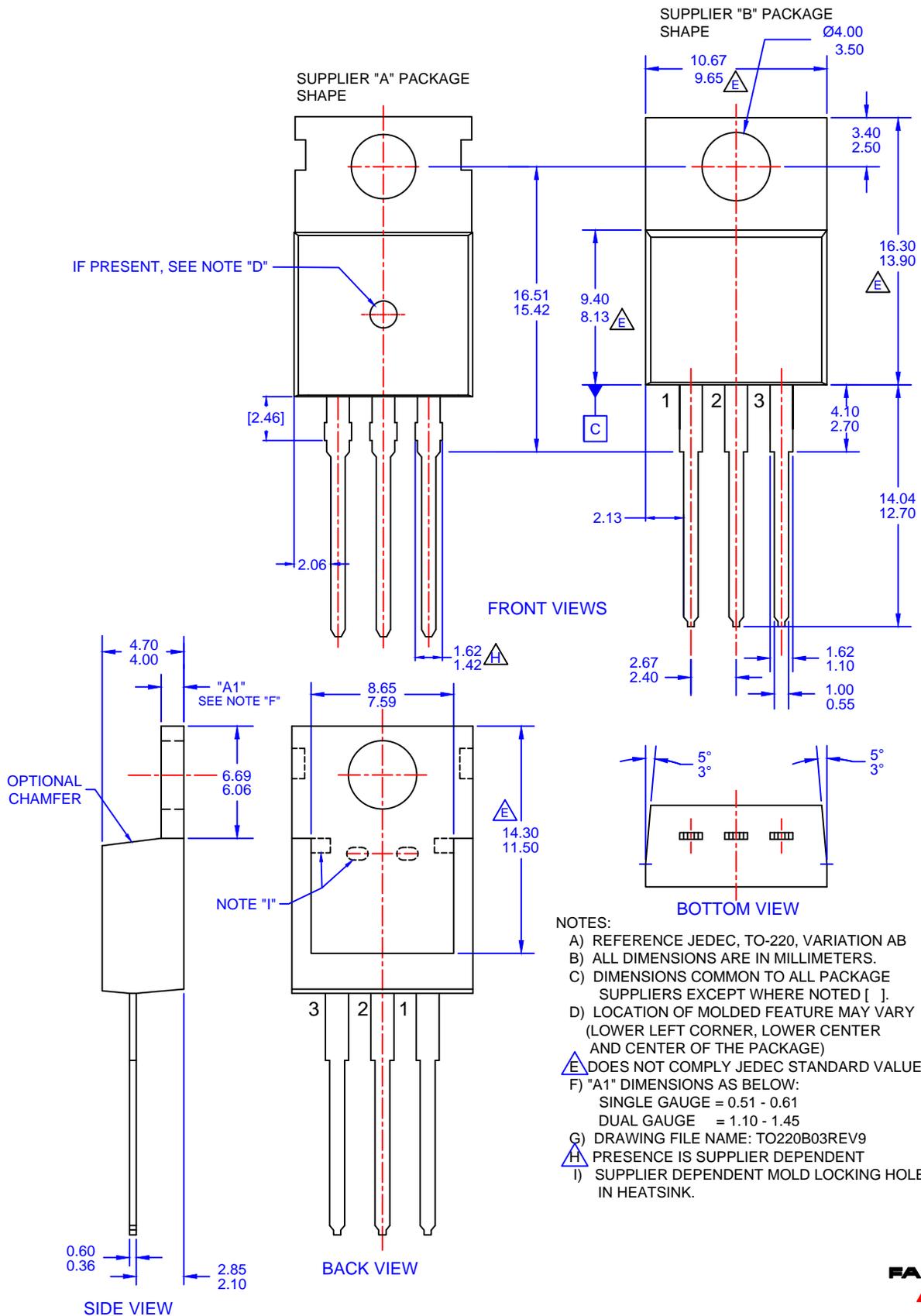
Figure 6. Power Derating



NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. FAIRCHILD SEMICONDUCTOR.
- F. DOES NOT COMPLY JEDEC STD VALUE.
- G. DRAWING FILE NAME: TO220U03REV1





- NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
 - D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
 - E) DOES NOT COMPLY JEDEC STANDARD VALUE.
 - F) "A1" DIMENSIONS AS BELOW:
 SINGLE GAUGE = 0.51 - 0.61
 DUAL GAUGE = 1.10 - 1.45
 - G) DRAWING FILE NAME: TO220B03REV9
 - H) PRESENCE IS SUPPLIER DEPENDENT
 - I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.



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