

# FQP2P40

## P-Channel QFET® MOSFET

-400 V, -2.0 A, 6.5 Ω

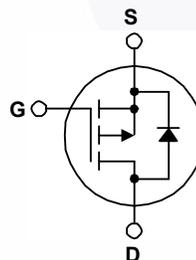
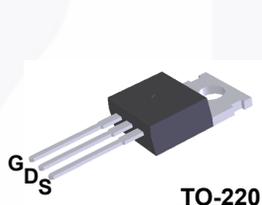
### Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp ballast based on complimentary half bridge.

### Features

- -2.0 A, -400 V,  $R_{DS(on)} = 6.5 \Omega$  (Max.) @  $V_{GS} = -10 V$
- Low Gate Charge (Typ. 10 nC)
- Low Crss (Typ. 6.5 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	FQP2P40_F080	Unit
V <sub>DSS</sub>	Drain-Source Voltage	-400	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)	-2.0	A
	- Continuous (T <sub>C</sub> = 100°C)	-1.27	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	-8.0	A
V <sub>GSS</sub>	Gate-Source Voltage	± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	120	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	-2.0	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	6.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C)	63	W
	- Derate Above 25°C	0.51	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	FQP2P40_F080	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case, Max.	1.98	°C/W
R <sub>θCS</sub>	Thermal Resistance, Case-to-Sink, Typ.	0.5	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP2P40_F080	FQP2P40	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-400	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	-	--	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -400\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -320\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.0\text{ A}$	--	5.0	6.5	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -1.0\text{ A}$	--	1.42	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	270	350	pF
$C_{oss}$	Output Capacitance		--	45	60	pF
$C_{rss}$	Reverse Transfer Capacitance		--	6.5	8.5	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -200\text{ V}, I_D = -2.0\text{ A},$ $V_{GS} = -10\text{ V}, R_G = 25\ \Omega$	--	9	30	ns	
$t_r$	Turn-On Rise Time		--	33	75	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	22	55	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	25	60	ns
$Q_g$	Total Gate Charge	$V_{DS} = -320\text{ V}, I_D = -2.0\text{ A},$ $V_{GS} = -10\text{ V}$	--	10	13	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4)	--	2.1	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	5.5	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	-2.0	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-8.0	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.0\text{ A}$	--	--	-5.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -2.0\text{ A},$	--	250	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	0.85	--	$\mu\text{C}$

#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = 52.5\text{ mH}, I_{AS} = -2.0\text{ A}, V_{DD} = -50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq -2.0\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Performance Characteristics

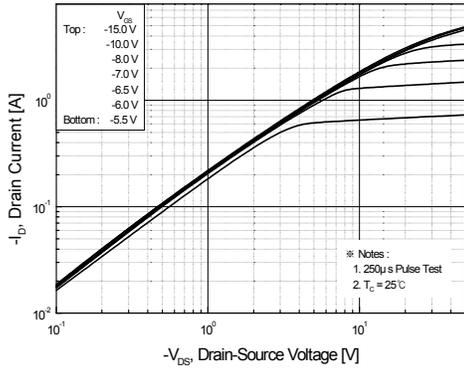


Figure 1. On-Region Characteristics

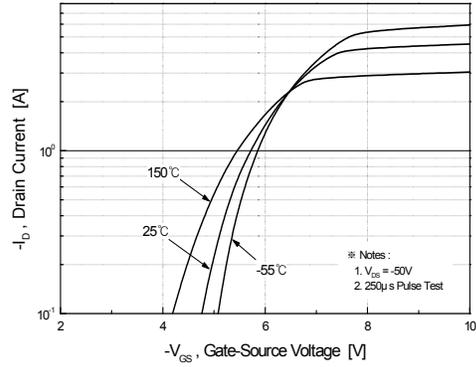


Figure 2. Transfer Characteristics

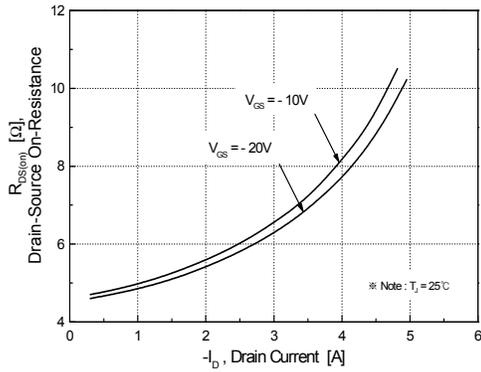


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

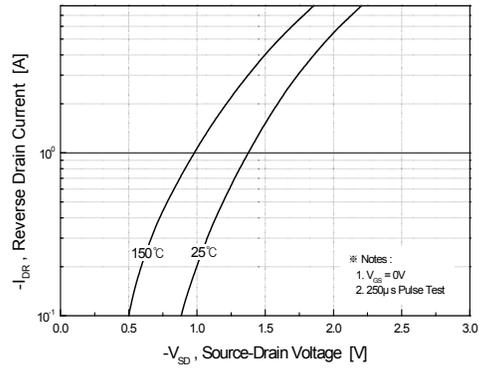


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

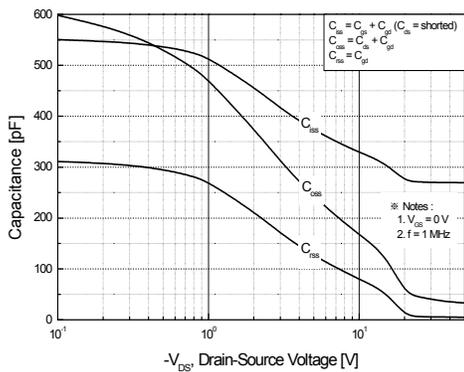


Figure 5. Capacitance Characteristics

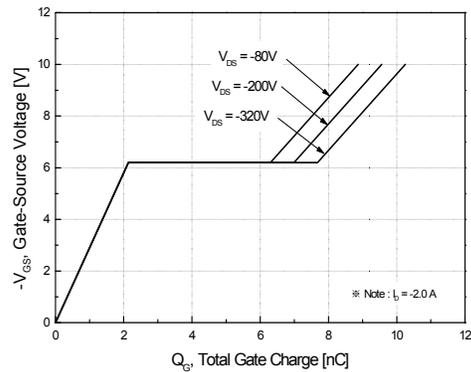
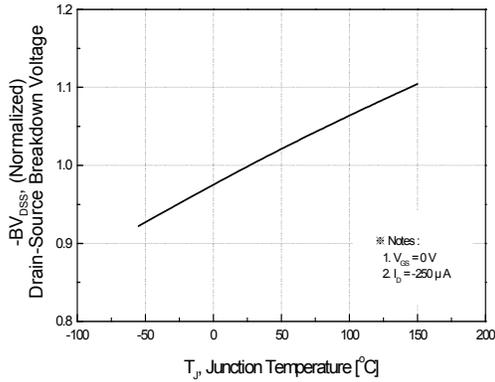
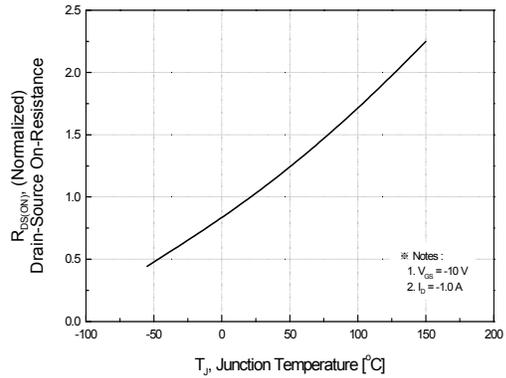


Figure 6. Gate Charge Characteristics

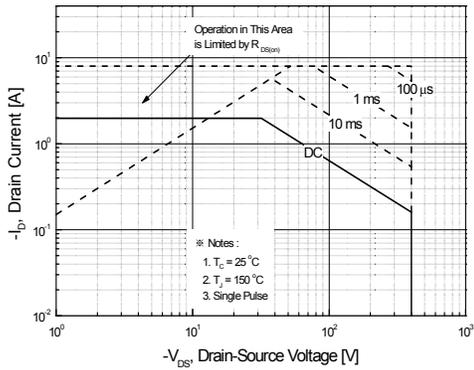
**Typical Performance Characteristics** (Continued)



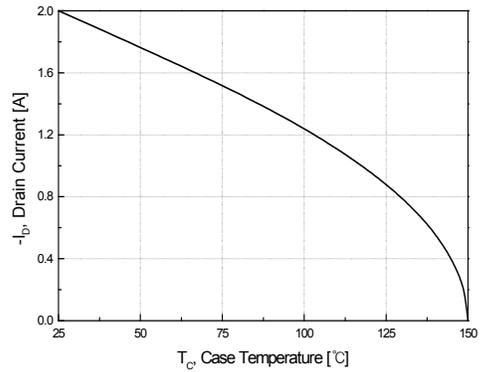
**Figure 7. Breakdown Voltage Variation vs. Temperature**



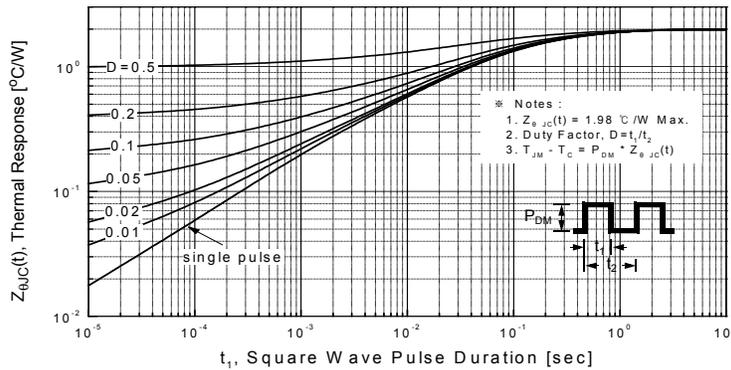
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

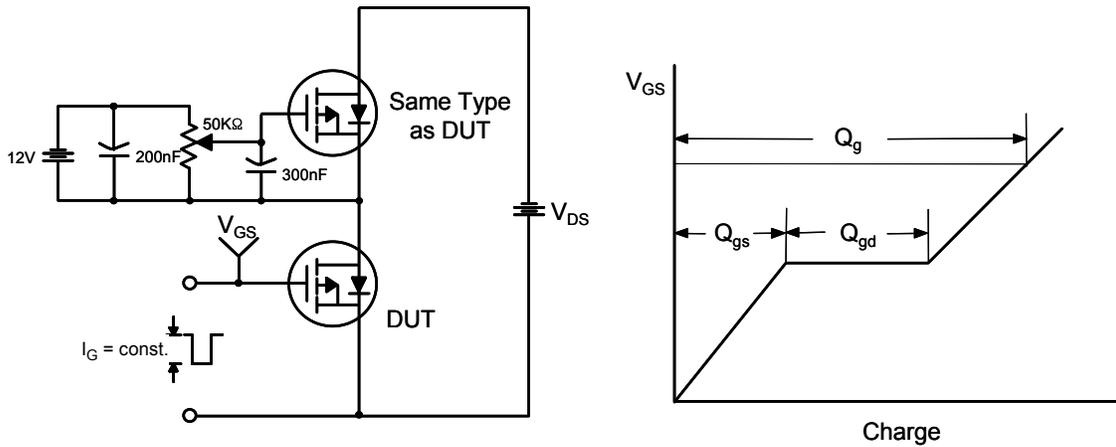


Figure 12. Gate Charge Test Circuit & Waveform

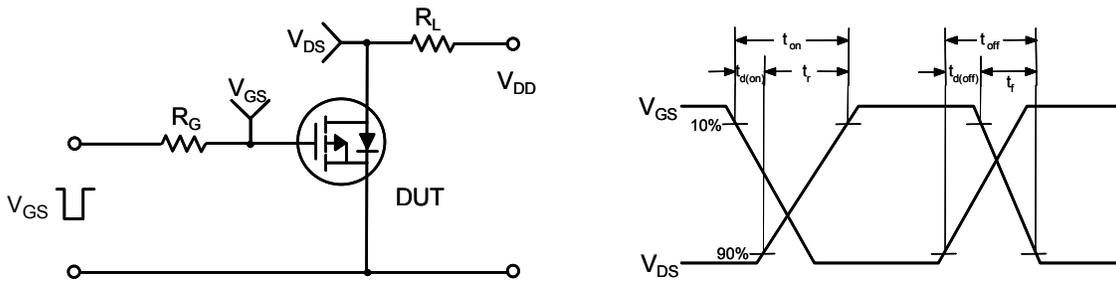


Figure 13. Resistive Switching Test Circuit & Waveforms

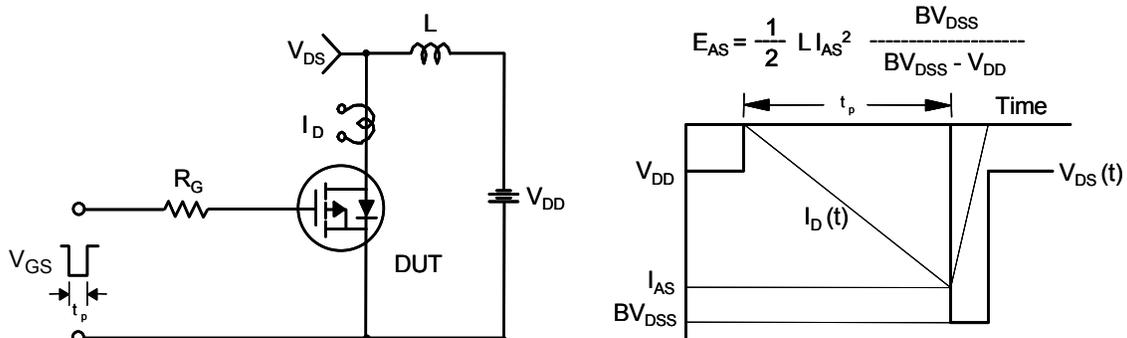


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

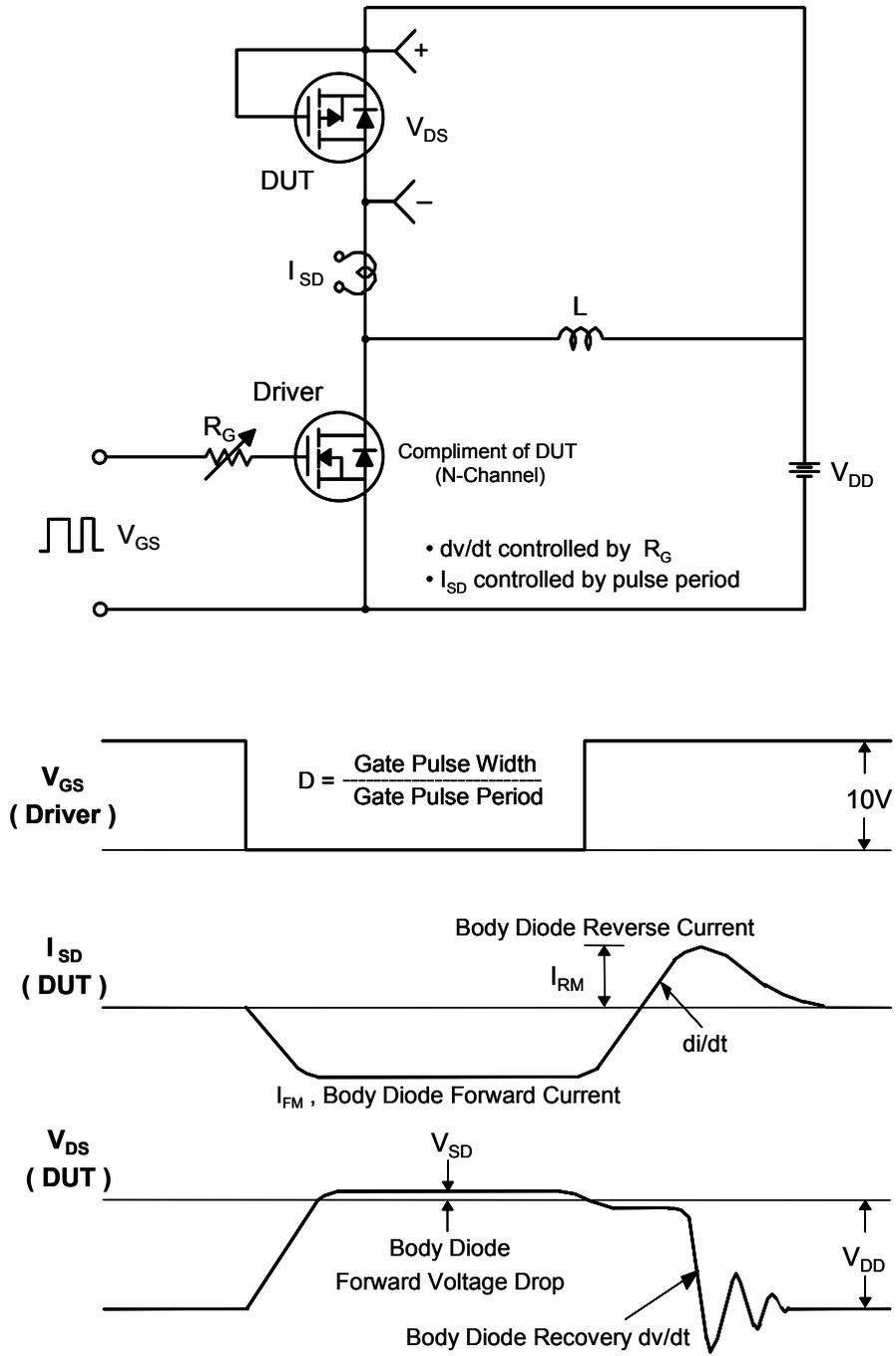
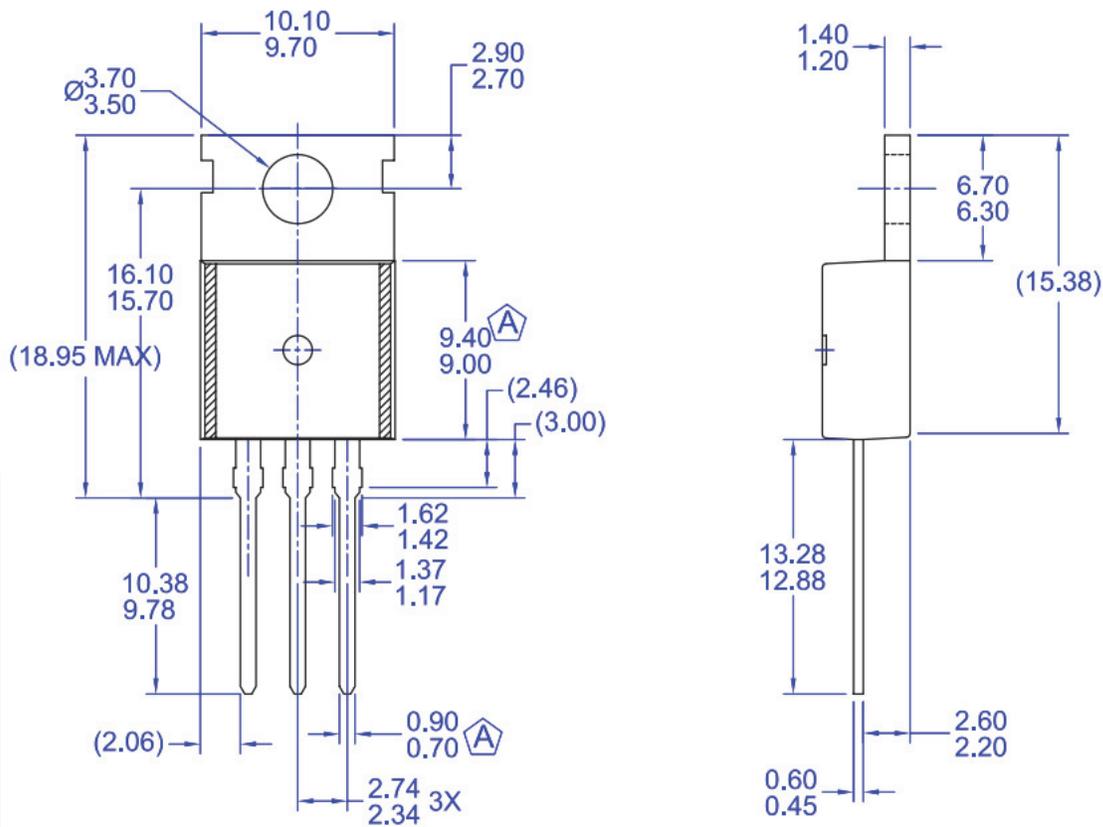


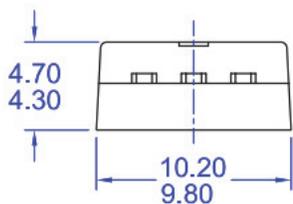
Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

### Mechanical Dimensions



**NOTES:**

- Ⓐ CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1



**Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

[http://www.fairchildsemi.com/package/packageDetails.html?id=PN\\_TO220-003](http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TO220-003)



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor:](#)

[FQP2P40\\_F080](#)