CapSense® Express™ Controllers with SmartSense™ Auto-tuning 16 Buttons, 2 Sliders, Proximity Sensors

The CY8CMBR3xxx CapSense® Express™ controllers enable advanced, yet easy-to-implement, capacitive touch sensing user interface solutions. This register-configurable family, which supports up to 16 capacitive sensing inputs, eliminates time-consuming firmware development. These controllers are ideal for implementing capacitive buttons, sliders, and proximity sensing solutions with minimal development-cycle times.

The CY8CMBR3xxx family features an advanced analog sensing channel and the Capacitive Sigma Delta PLUS (CSD PLUS) sensing algorithm, which delivers a signal-to-noise ratio (SNR) of greater than 100:1 to ensure touch accuracy even in extremely noisy environments. These controllers are enabled with Cypress's SmartSense™ Auto-tuning algorithm, which compensates for manufacturing variations and dynamically monitors and maintains optimal sensor performance in all environmental conditions. In addition, SmartSense Auto-tuning enables a faster time-to-market by eliminating the time-consuming manual tuning efforts during development and production ramp-up.

Advanced features, such as LED brightness control, proximity sensing, and system diagnostics, save development time. These controllers enable robust liquid-tolerant designs by eliminating false touches due to mist, water droplets, or streaming water. The CY8CMBR3xxx controllers are offered in a variety of small form factor industry-standard packages.

The ecosystem for the CY8CMBR3xxx family includes development tools—software and hardware—to enable rapid user interface designs. For example, the EZ-Click Customizer tool is a simple graphical user interface software for configuring the device features through the I^2C interface. This tool also supports CapSense data viewing to monitor system performance and support validation and debugging. Another tool, the Design Toolbox, simplifies circuit board layout by providing design guidelines and layout recommendations to optimize sensor size, trace lengths, and parasitic capacitance. To quickly evaluate the CY8CMBR3xxx family features, use the CY3280-MBR3 Evaluation Kit.

- Register-configurable CapSense Express controller
  - No firmware development required
  - Patented CSD sensing algorithm
  - High sensitivity (0.1 pF)
    - Overlay thickness of up to 15 mm for glass and 5 mm for plastic
    - Proximity solutions
    - Sensitivity up to 2 fF per count
  - Best-in-class >100:1 SNR performance
    - Superior noise-immunity performance against conducted and radiated noise
    - Ultra-low radiated emissions
  - SmartSense Auto-tuning
    - Sets and maintains optimal sensor performance during run time
    - Eliminates manual tuning during development and production
- Low-power CapSense
  - Average current consumption of 22 µA per sensor at 120-ms refresh interval
  - Wide parasitic capacitance (C_P) range: 5–45 pF
- Advanced user interface features
  - Liquid tolerance
  - User-configurable LED brightness for visual touch feedback
    - Up to eight high-sink current GPOs to drive LEDs
  - Buzzer signal output for audible touch feedback
  - Flanking Sensor Suppression (FSS) to eliminate false touches in closely spaced buttons
  - Analog voltage output
  - Attention line interrupt to the host to indicate any change in sensor status
- System diagnostics to detect
  - Improper value of the modulating capacitor (CMOD)
  - Out of range sensor parasitic capacitance (C_P)
  - Sensor shorts
- EZ-Click™ Customizer tool
  - Simple GUI for device configuration
  - Data viewing and monitoring for CapSense buttons, sliders, and proximity sensors
  - System diagnostics for rapid debug
- I^2C slave
  - Supports up to 400 kHz
  - Wake-on-hardware address match
  - No bus-stalling or clock-stretching during transactions
- Low-power 1.71-V to 5.5-V operation
  - Deep Sleep mode with wake-up on interrupt and I^2C address detect
- Industrial temperature range: –40 °C to +85 °C
- Package options
  - 8-pin SOIC (150 mil)
  - 16-pin SOIC (150 mil)
  - 16-pin QFN (3 × 3 × 0.6 mm)
  - 24-pin QFN (4 × 4 × 0.6 mm)

Cypress provides a wealth of data at www.cypress.com to help you to select the right CapSense device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4.

Cypress provides a complete ecosystem to enable a quick development cycle with the CY8CMBR3xxx CapSense controller family. This ecosystem includes simple tools for device configuration, design validation, and diagnostics.

Design Guides

Design guides are an excellent introduction to a variety of possible CapSense-based designs. They provide an introduction to the solution and complete system design guidelines. Refer to the following design guides for CY8CMBR3xxx:

1. Getting Started with CapSense – an ideal starting point for all CapSense users
2. CY8CMBR3xxx CapSense Design Guide – provides complete system design guidelines for CY8CMBR3xxx

You can download these design guides from our website: www.cypress.com/go/capsense.

Registers TRM

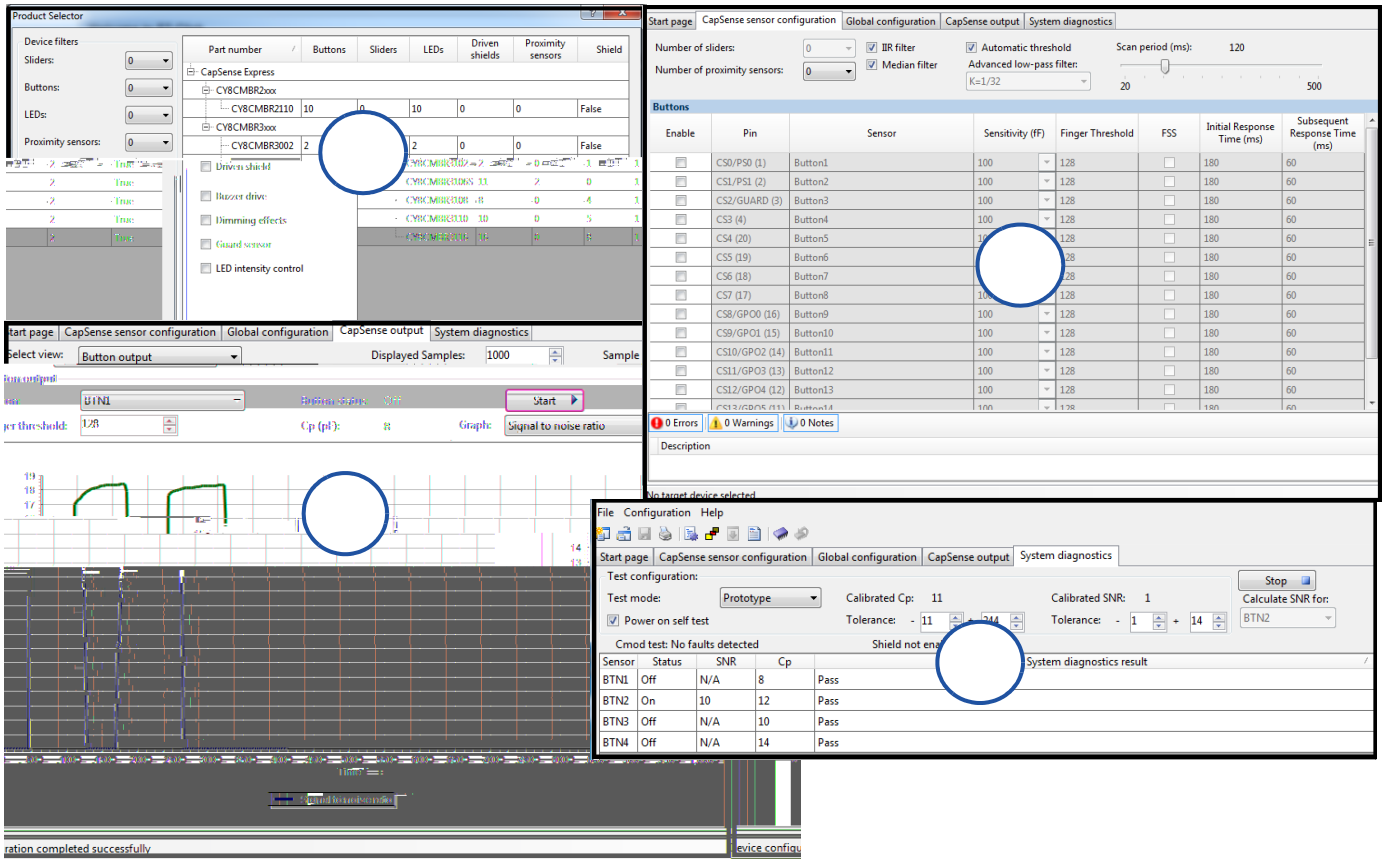
The CY8CMBR3xxx Registers TRM lists and details all the registers of the CY8CMBR3xxx family of controllers in order of their addresses. These registers may be accessed through an I^2C interface with the host.

EZ-Click Customizer Tool

The EZ-Click Customizer Tool is a simple, GUI-based software utility that can be used to customize the CY8CMBR3xxx device configurations.

Use this GUI-based tool to do the following:

1. Select the appropriate part number based on an end-application requirement using the Product Selector
2. Configure the device features
3. Observe CapSense data for button and proximity sensors
4. Use the System Diagnostics and built-in test self-test (BIST) features for debug and production-line testing



The Design Toolbox is an interactive spreadsheet tool that provides application-specific design guidelines for capacitive buttons. It is used to configure and validate the CapSense system.

The Design Toolbox:

- Provides general layout guidelines for a CapSense PCB
- Estimates button dimensions based on end-application requirements
- Calculates power consumption based on button dimensions
- Validates layout design

The CY3280-MBR3 Evaluation Kit can be used to quickly evaluate the various features of the CY8CMBR3xxx solution. The kit also functions as an Arduino shield, making it compatible with the various Arduino-based controllers in the market. You can purchase this kit at the Cypress online store.

In addition to print documentation, there are abundant web resources. The dedicated web page for the CY8CMBR3xxx family has all the current information.

Free PSoC and CapSense technical training (on-demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and supports different skill levels to assist you in your designs.

For assistance with technical issues, search the Knowledge Base articles and forums at www.cypress.com/support. If you cannot find an answer to your question, create a technical support case or call technical support at 1-800-541-4736.

CapSense Sensors 6
Sliders 6
Proximity Sensors 6
SmartSense Auto-tuning 6
Liquid Tolerance 6
Noise Immunity 6
Flanking Sensor Suppression (FSS) 6
Touch Feedback 6
General-Purpose Outputs (GPOs) 6
Buzzer Drive 6
Register Configurability 7
Communication to Host 7
System Diagnostics 7
Ultra-Low Power Consumption 7
MPN versus Features Summary 8

CY8CMBR3116 (16 Sensing Inputs) 9
CY8CMBR3106S (16 Sensing Inputs; Sliders Supported) 11
CY8CMBR3108 (8 Sensing Inputs) 12
CY8CMBR3110 (10 Sensing Inputs) 13
CY8CMBR3102 (2 Sensing Inputs) 14
CY8CMBR3002 (2 Sensing Inputs) 14
Unused SPO Pin Connection 15
Unused SPO Pin Connection for AXRES pins 15
Unused GPO Pin Connection 15

Automatic Threshold 16
Sensitivity Control 16
Sensor Auto Reset 16
Noise Immunity 17
Flanking Sensor Suppression 17
General-Purpose Outputs 17
LED ON Time 18
Toggle 18
Buzzer Signal Output 18
Host Interrupt 19
Latch Status Output 19
Analog Voltage Output 19
System Diagnostics 20

Absolute Maximum Ratings 24
Operating Temperature 24
DC Electrical Characteristics 24
AC Electrical Specifications 25
I2C Specifications 26

I2C Slave Address 31
I2C Communication Guidelines 32
Write Operation 32
Setting the Device Data Pointer 32
Read Operation 33

Ordering Code Definitions 34

Thermal Impedances 37
Solder Reflow Specifications 37

Units of Measure 38

Worldwide Sales and Design Support 42
Products 42
PSoC® Solutions 42
Cypress Developer Community 42
Technical Support 42

A capacitive sensor detects changes in capacitance to determine the presence of a touch or proximity to conductive objects. The capacitive sensor can be a capacitive button that replaces the traditional mechanical buttons, a capacitive slider that replaces mechanical knobs, or a proximity sensor that replaces an infrared sensor in a user interface solution. A typical capacitive user interface system consists of the following:

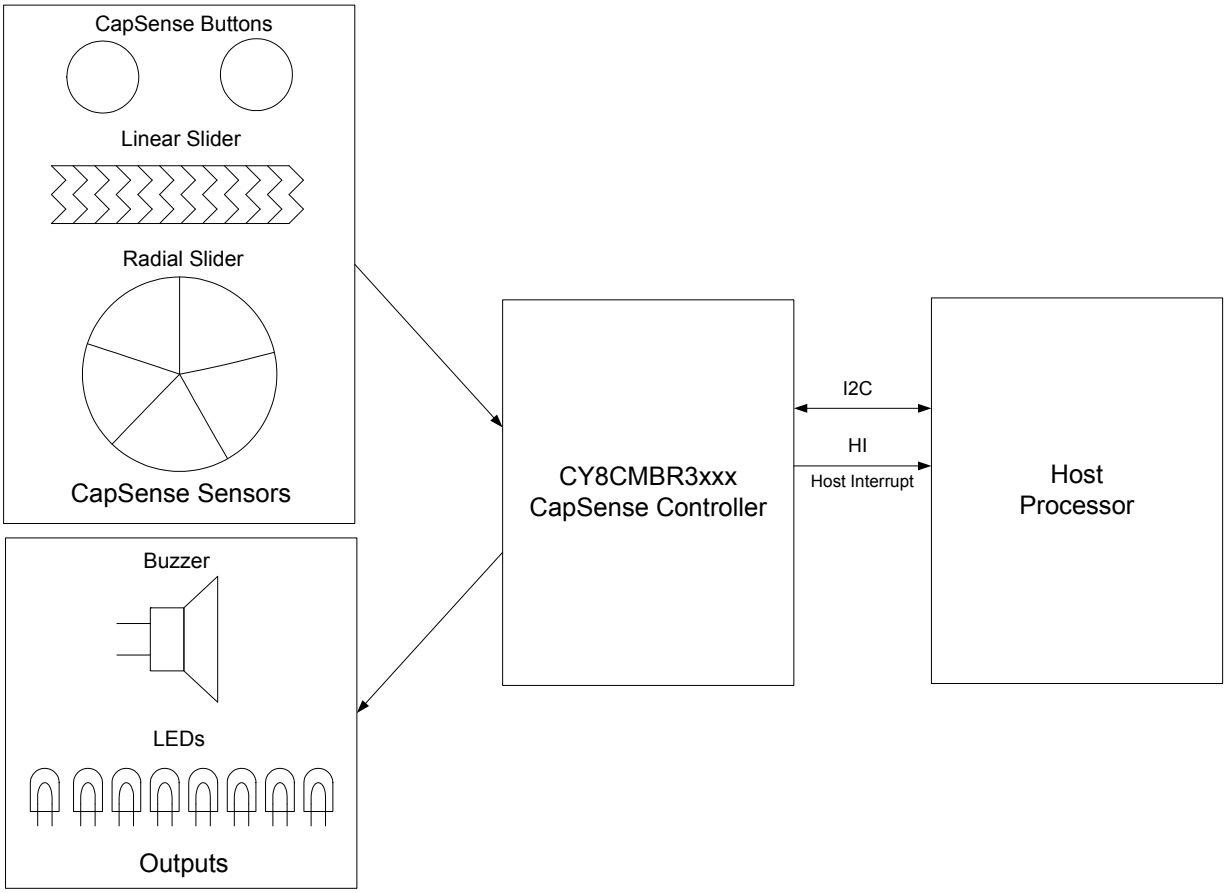
- A capacitive sensor
- An audio-visual output, such as a buzzer or an LED
- A capacitive sensing controller connected to the sensor
- A host processor

The capacitive controller connects the sensor and the output to the host processor through a communication interface, such as an I^2C or a GPO.

The capacitive user interface system serves as a human-machine interface that takes the user's touch inputs and provides audio-visual feedback through a buzzer or an LED. CY8CMBR3xxx is a family of capacitive sensing controllers, which senses the change in capacitance based on touch or proximity, and controls the user interface system accordingly. The sensing algorithm, built in the controllers, determines the presence of touch and drives the outputs or sends signals to the host processor. This algorithm can distinguish between the signal (based on touch or proximity) and noise, which can be caused by environmental or electrical conditions.

Figure 2 shows a typical user interface system with capacitive buttons connected to a CY8CMBR3xxx CapSense Express controller, which controls the system and also communicates with the host processor through I^2C.

Traditionally, capacitive sensing controllers require firmware development to perform specific user interface functions and manual system tuning to achieve optimal performance. However, the CY8CMBR3xxx CapSense Express family of controllers does not require any firmware development, accelerating time-to-market. These devices feature SmartSense Auto-tuning, which eliminates the need for manual tuning, providing optimal performance even under extremely noisy conditions.



The CY8CMBR3xxx family of controllers supports up to 16 capacitive sensors. These can be configured as follows:

- Up to 16 CapSense buttons
- Up to two sliders: Configurable as linear or radial sliders
- Up to two proximity sensors that can detect up to 30-cm proximity distance

- Supports up to two 5-segment sliders
- Configures each slider individually as linear or radial
- Combines both sliders to form one 10-segment slider
- Slider resolution is user-configurable

- The CY8CMBR3xxx family supports up to two proximity sensors with a detection range of up to 30 cm. These proximity sensors are capable of detecting both proximity and touch events.
- The wake-on-approach feature wakes the devices from a low-power state to Active mode on a proximity event.
- The device also features driven shield, which enhances the proximity sensing range in the presence of metal objects.
- The device supports proximity sensors with C_P ranging from 8 pF to 45 pF.

The CY8CMBR3xxx family features SmartSense Auto-tuning, Cypress's patented CapSense algorithm, which continuously compensates for system and environmental changes during run time. SmartSense Auto-tuning has the following advantages:

- Reduces design effort by eliminating manual tuning
- Adapts to variations in PCB, overlay, paint, and manufacturing that degrade touch-sensing performance
- Eliminates manual tuning in production
- Adapts to changes in the system environment due to noise
- Allows a platform design approach with different overlays, button shapes, and trace lengths

The CY8CMBR3xxx family delivers water-tolerant designs that eliminate false touches due to wet conditions, such as water droplets, moisture, mist, steam, or even wet hands. The CapSense controller locks up the user interface in firmware to prevent touch inputs in streaming water.

The CY8CMBR3xxx family offers liquid-tolerance to liquids such as water, ketchup, oil, and blood.

Enable the shield electrode through the register map, using EZ-Click, to prevent false touches under wet conditions and enable both the shield electrode and guard sensor to prevent false touches in streaming water conditions. The shield electrode and guard sensor consume a port pin each in the CapSense controller. Refer to the CY8CMBR3xxx CapSense Design Guide for best practices and design guidelines for implementing liquid-tolerant designs.

The CY8CMBR3xxx family features the robust CSD PLUS capacitive sensing algorithm. Additionally, it implements the advanced noise immunity algorithm, EMC, for stable operation in extremely noisy conditions.

The EMC algorithm has higher average power consumption. For low-power applications, where noise conditions are not extreme, you can disable this feature through the I^2C interface.

This feature distinguishes between signals from closely spaced buttons, eliminating false touches. It ensures that the system recognizes only the first button touched.

The CY8CMBR3xxx family has pins that you can configure for audio-visual feedback through a buzzer or an LED.

The GPOs are high-sink current outputs that can drive most LEDs. The GPO status can be controlled directly by the CapSense sensors so that a sensor 'ON' status automatically turns ON a corresponding LED. Alternatively, GPOs can be controlled by the host through the I^2C interface.

The GPOs also support advanced features, such as:

- CSx to GPOx Direct Drive: Directly control the GPOs upon button touch or proximity event.
- Pulse width modulation (PWM): Controls LED brightness.
- Toggle: The GPO status is toggled upon every touch event on the button sensors, and proximity event on proximity sensors, to mimic the functionality of the mechanical toggle switch.
- Voltage output: Analog voltage that represents the button status.

The output pins of the CY8CMBR3xxx controllers can be configured for driving a single-input DC Piezo-electric buzzer through a PWM. The PWM frequency and buzzer activation duration are configurable. The buzzer output is activated for a finite amount of time when a finger touch is detected.

The CY8CMBR3xxx registers may be configured through the I^2C interface. Device features may be enabled, disabled, or modified by writing appropriate values to the I^2C configurable register map. This register map also provides various status outputs to indicate the touch/release status and system performance and debug parameters.

You can access the register map of the device through the I^2C interface by a host controller, such as a microcontroller or the EZ-Click Customizer.

The CY8CMBR3xxx devices feature a safe register map update mechanism to overcome configuration data corruption, which can occur due to power failure during flash writes or any other spurious events. If the configuration data is corrupted during a register map update, the devices reconfigure themselves to the last known valid configuration.

The CY8CMBR3xxx family communicates to a host processor through the following methods:

- The I^2C interface allows the host to configure parameters and receive status information on touch events
- The host interrupt alerts the host when a new touch event occurs. This helps to build effective communication between the host and the CapSense controller. Alternatively, the CPU can poll the device status by reading through I^2C.
- The GPO provides the ON or OFF sensor status to the host. The GPO ports can also be used to implement analog voltage and DC output (DCO) using an external resistor network.

The CY8CMBR3xxx devices are equipped with a system diagnostics feature to detect system-level fault conditions and to avoid failure of the user interface design. The system diagnostic features also help to monitor system-level parameters to debug the design during development.

The built-in system diagnostics detects the following fault conditions at power-up and helps to monitor the following:

- Improper value of the modulating capacitor (C_{MOD})
- C_P value out of range
- Sensor shorts

For low-power applications, such as those operated by a battery, select a capacitive sensing controller that has ultra-low average power consumption.

The CY8CMBR3xxx controllers draw an average current of 22 µA per sensor at 1.8 V.

The CY8CMBR3xxx family supports two operating modes:

- Active: The sensors are scanned periodically for power optimization.
- Deep Sleep: The sensors are not scanned until a command from the host is received to resume sensor scanning.

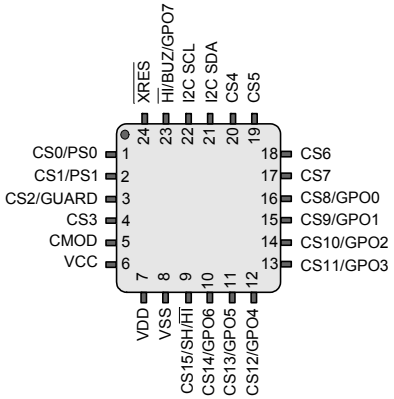
In the Active mode, CY8CMBR3xxx family implements additional techniques, such as optimizing the average power consumption and providing a smooth user interface experience without increasing the refresh interval.

In addition to these modes, the device has a wake-on approach feature, which uses proximity sensing to reduce the average power consumption, ensuring power saving when the system is inactive.

Details of all features are documented in Device Feature Details on page 16.

The CY8CMBR3xxx family consists of six MPNs, each MPN supporting a different feature set. The following table lists all MPNs and a summary of the features supported by each.

1	Maximum number of buttons	16	11	10	8	2	2
2	Maximum number of sliders	×	2	×	×	×	×
3	Maximum number of proximity sensors	2	2	2	2	2	×
4	Shield electrode	✔	✔	✔	✔	✔	×
5	Guard Sensor	✔	×	✔	✔	×	×
6	Wake-on-approach	✔	✔	✔	✔	✔	×
7	Liquid tolerance	✔	×	✔	✔	✔	×
8	Automatic threshold	✔ Configurable	✔ Configurable	✔ Configurable	✔ Configurable	✔ Configurable	✔
9	Threshold Override	×	✔	×	✔	✔	×
10	Sensitivity Control	✔	✔	✔	✔	✔	×
11	Sensor auto-reset	✔	✔	✔	✔	✔	✔ 20s
12	Median & IIR filter	✔	✔	✔	✔	✔	✔
13	Advanced-Low-Pass Filter	✔	×	✔	✔	✔	×
14	Electromagnetic Compatibility (EMC)	✔	✔	✔	✔	✔	×
15	FSS	✔	✔	✔	✔	✔	×
16	Maximum number of GPOs/LED drive outputs	8	0	5	4	1	2
17	GPO/LED Sink and Source Drive Support	✔ Configurable	×	✔ Configurable	✔ Configurable	✔ Configurable	Sink
18	LED brightness control	✔	×	✔	✔	✔	×
19	LED ON time	✔	×	✔	✔	✔	×
20	Toggle	✔	×	✔	✔	✔	×
21	Buzzer Signal Output	✔	✔	✔	✔	×	×
22	Host interrupt	✔	✔	✔	✔	×	×
23	Latch Status Output	✔	✔	✔	✔	✔	×
24	Analog Voltage Output	✔	×	✔	✔	✔	✔
25	System diagnostics	✔	✔	✔	✔	✔	✔
26	I^2C Interface	✔	✔	✔	✔	✔	×

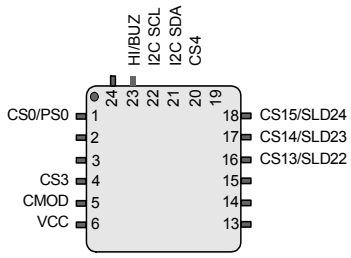
1	CS0/PS0	–	CapSense button / proximity sensor, controls GPO0	Ground/Ground	CS0	
2	CS1/PS1	–	CapSense button / proximity sensor, controls GPO1	Ground/Ground	CS1	
3	CS2/GUARD	–	CapSense button / guard sensor, controls GPO2	Ground/Ground	CS2	
4	CS3	–	CapSense button, controls GPO3	Ground	CS3	
5	CMOD	–	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	CMOD	
6	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD.	NA	VCC	
7	VDD	Power	Power	NA	VDD	
8	VSS	Power	Ground	NA	VSS	
9	CS15/SH/$\overline{HI}$	I/DO	CapSense button / shield electrode/ Host Interrupt (SPO1 in the register map)	Refer to Unused SPO Pin Connection on page 15	$\overline{HI}$	

(continued)

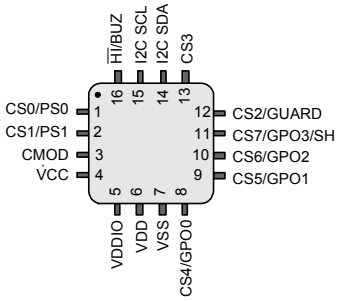
10	CS14/GPO6	I/DO	CapSense button / general purpose output (GPO)	Ground/Refer to Unused GPO Pin Connection on page 15	GPO6	
11	CS13/GPO5	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO5	
12	CS12/GPO4	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO4	
13	CS11/GPO3	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO3	
14	CS10/GPO2	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO2	
15	CS9/GPO1	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO1	
16	CS8/GPO0	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO0	
17	CS7	–	CapSense button, controls GPO7	Ground	CS7	
18	CS6[2]	–	CapSense button, controls GPO6	Connect to VDD	CS6	
19	CS5	–	CapSense button, controls GPO5	Ground	CS5	
20	CS4	–	CapSense button, controls GPO4	Ground	CS4	
21	I2C SDA	DIO	I2C data	Pull up	I2C SDA	
22	I2C SCL	DIO	I2C clock	Pull up	I2C SCL	
23	$\overline{\text{HI}}$/BUZ/ GPO7	DO	Host Interrupt / buzzer output / GPO (SPO0 in the register map)	Refer to Unused SPO Pin Connection on page 15	GPO7	
24	$\overline{\text{XRES}}$	$\overline{\text{XRES}}$	Active Low external reset (an active low pulse on this pin resets the CapSense Controller)	Leave open	$\overline{\text{XRES}}$	
25	Center Pad[1]	E-pad	Connect to VSS for best mechanical, thermal, and electrical performance	Floating, not connected to any other signal	E-pad	

: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, DO = Digital Output, CS = CapSense Button, PS = Proximity Sensor
SH = Shield Electrode, BUZ = Buzzer Output, GPO = General Purpose Output, GUARD = Guard Sensor, SPO = Special purpose output.

1. The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If it is not connected to ground, it should be left floating without being connected to any other signal.
2. This I/O functions as reset ($\overline{\text{AXRES}}$) pin during boot-up. Make certain that this pin is not grounded during power-up for the device to boot up properly. After boot-up, this I/O functions as indicated by the pin name.

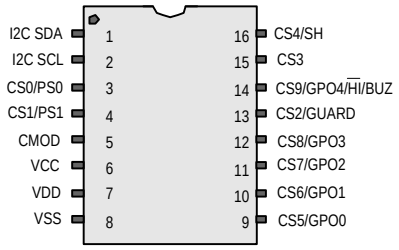
1	CS0/PS0	–	CapSense button / proximity sensor	Ground/Ground	CS0	
2	CS1/PS1	–	CapSense button / proximity sensor	Ground/Ground	CS1	
3	CS2	–	CapSense button	Ground	CS2	
4	CS3	–	CapSense button	Ground	CS3	
5	CMOD	–	External modulator capacitor. Connect 2.2 nF/ 5 V/X7R or NPO capacitor	NA	CMOD	
6	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD.	NA	VCC	
7	VDD	Power	Power	NA	VDD	
8	VSS	Power	Ground	NA	VSS	
9	SLD10	–	Slider1, segment0	Ground	SLD10	
10	SLD11	–	Slider1, segment1	Ground	SLD11	
11	SLD12	–	Slider1, segment2	Ground	SLD12	
12	SLD13	–	Slider1, segment3	Ground	SLD13	
13	SLD14	–	Slider1, segment4	Ground	SLD14	
14	CS11/SLD20	–	CapSense button / Slider2, segment0	Ground/Ground	SLD20	
15	CS12/SLD21	–	CapSense button / Slider2, segment1	Ground/Ground	SLD21	
16	CS13/SLD22	–	CapSense button / Slider2, segment2	Ground/Ground	SLD22	
17	CS14/SLD23	–	CapSense button / Slider2, segment3	Ground/Ground	SLD23	
18	CS15/SLD24[4]	–	CapSense button / Slider2, segment4	Connect to VDD/Connect to VDD	SLD24	
19	CS5/SH/$\overline{HI}$	–	CapSense button / shield electrode/host interrupt. (SPO1 in the register map)	Refer to Unused SPO Pin Connection on page 15	CS5	
20	CS4	–	CapSense Button	Ground	CS4	
21	I2C SDA	DIO	I2C Data	Pull up	I2C SDA	
22	I2C SCL	DIO	I2C Clock	Pull up	I2C SCL	
23	$\overline{HI}$/BUZ	O	Host interrupt / buzzer output. This pin acts as SPO0 for this device (SPO0 in register map).	Refer to Unused SPO Pin Connection on page 15	$\overline{HI}$	
24	$\overline{XRES}$	$\overline{XRES}$	External reset	Leave open	$\overline{XRES}$	
25	Center Pad[3]	$\overline{E\text{-}pad}$	Connect to VSS for best mechanical, thermal and electrical performance	Floating, not connected to any other signal	E-pad	

: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, CS = CapSense Button, PS = Proximity Sensor, SH = Shield Electrode, BUZ = Buzzer Output, SPO = Special Purpose Output.

1	CS0/PS0	–	CapSense button / proximity sensor, controls GPO0	Ground/Ground	CS0	
2	CS1/PS1	–	CapSense button / proximity sensor, controls GPO1	Ground/Ground	CS1	
3	CMOD	–	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	CMOD	
4	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD	NA	VCC	
5	VDDIO	Power	Power for I2C and $\overline{HI}$ lines	Connect to VDD	VDDIO	
6	VDD	Power	Power	NA	VDD	
7	VSS	Power	Ground	NA	VSS	
8	CS4/GPO0	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO0	
9	CS5/GPO1	–	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO1	
10	CS6/GPO2	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO2	
11	CS7/GPO3/ SH	I/DO	CapSense button / GPO/ shield electrode. (SPO1 in the register map)	Refer to Unused SPO Pin Connection on page 15	GPO3	
12	CS2/GUARD[6]	–	CapSense button, controls GPO2 / guard sensor	Connect to VDD/Connect to VDD	CS2	
13	CS3	–	CapSense button, controls GPO3	Ground	CS3	
14	I2C SDA	DIO	I2C data	Pull up	I2C SDA	
15	I2C SCL	DIO	I2C clock	Pull up	I2C SCL	
16	$\overline{HI}$/BUZ	DO	Host interrupt / buzzer output Supply voltage for buzzer and pull-up resistor on $\overline{HI}$ should be equal to VDDIO (SPO0 in the register map).	Refer to Unused SPO Pin Connection on page 15	$\overline{HI}$	
17	Center Pad[5]	E-pad	Connect to VSS for best mechanical, thermal and electrical performance	Floating, not connected to any other signal	E-pad	

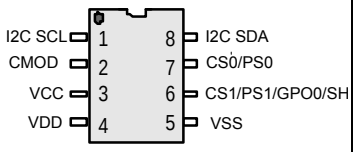
: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, CS = CapSense Button, PS = Proximity Sensor
SH = Shield Electrode, BUZ = Buzzer Output, GPO = General Purpose Output, GUARD = Guard Sensor, SPO = Special Purpose Output.

5. The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If it is not connected to ground, it should be left floating without being connected to any other signal.
6. This I/O functions as reset ($\overline{XRES}$) pin during boot-up. Make certain that this pin is not grounded during power-up for the device to boot up properly. After boot-up, this I/O functions as indicated by the pin name.

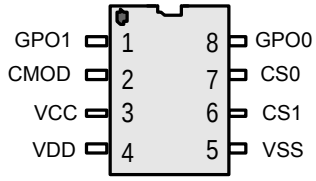
1	I2C SDA	DIO	I2C data	Pull up	I2C SDA	
2	I2C SCL	DIO	I2C clock	Pull up	I2C SCL	
3	CS0/PS0	–	CapSense button / proximity sensor, controls GPO0	Ground/Ground	CS0	
4	CS1/PS1	–	CapSense button / proximity sensor, controls GPO1	Ground/Ground	CS1	
5	CMOD	–	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	CMOD	
6	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD	NA	VCC	
7	VDD	Power	Power	NA	VDD	
8	VSS	Power	Ground	NA	VSS	
9	CS5/GPO0	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO0	
10	CS6/GPO1	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO1	
11	CS7/GPO2	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO2	
12	CS8/GPO3	I/DO	CapSense button / GPO	Ground/Refer to Unused GPO Pin Connection on page 15	GPO3	
13	CS2/GUARD	–	CapSense button, controls GPO2 / guard sensor	Ground/Ground	CS2	
14	CS9/GPO4/$\overline{\text{HI}}$/BUZ[7]	I/DO	CapSense button / GPO / host interrupt / buzzer output. (SPO1 in the register map)	Refer Unused SPO Pin Connection for AXRES pins on page 15	GPO4	
15	CS3	–	CapSense button, controls GPO3	Ground	CS3	
16	CS4/SH	I/O	CapSense button, controls GPO4 / shield electrode (SPO0 in the register map).	Refer to Unused SPO Pin Connection on page 15	CS4	

: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, CS = CapSense Button, PS = Proximity Sensor
SH = Shield Electrode, BUZ = Buzzer Output, GPO = General Purpose Output, GUARD = Guard Sensor, SPO = Special Purpose Output.

7. This I/O functions as reset ($\overline{\text{AXRES}}$) pin during boot-up. Make certain that this pin is not grounded during power-up for the device to boot up properly. After boot-up, this I/O functions as indicated by the pin name.

1	I2C SCL	DIO	I2C clock	Pull up	I2C SCL	
2	CMOD	–	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	CMOD	
3	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD.	NA	VCC	
4	VDD	Power	Power	NA	VDD	
5	VSS	Power	Ground	NA	VSS	
6	CS1/PS1/ GPO0/SH	I/DO/O	CapSense button / proximity sensor/ GPO/ shield electrode (SPO0 in the register map).	Refer to Unused SPO Pin Connection on page 15	GPO0	
7	CS0/PS0[8]	–	CapSense button / proximity sensor, controls GPO0	Connect to VDD/ Connect to VDD	CS0	
8	I2C SDA	DIO	I2C data	Pull up	I2C SDA	

I = Analog Input, O = Analog Output, DIO = Digital Input/Output, CS = CapSense Button, PS = Proximity Sensor, SH = Shield Electrode, GPO = General Purpose Output, SPO = Special Purpose Output.

1	GPO1	DO	Active-low GPO with open-drain-low drive mode	Ground	
2	CMOD	I/O	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	
3	VCC	Power	Internal regulator output. Connect a 0.1-µF decoupling capacitor if VDD > 1.8 V. If VDD is 1.71 V to 1.89 V, short this pin to VDD.	NA	
4	VDD	Power	Power	NA	
5	VSS	Power	Ground	NA	
6	CS1	–	CapSense button, controls GPO1	Ground	
7	CS0[8]	–	CapSense button, controls GPO0	Connect to VDD	
8	GPO0	DO	Active-low GPO with open-drain-low drive mode	Ground	

Legend: I = Analog Input, DO = Digital Output, CS = CapSense Button, GPO = General Purpose Output

8. This I/O functions as reset ($\overline{\text{AXRES}}$) pin during boot-up. Make certain that this pin is not grounded during power-up for the device to boot up properly. After boot-up, this I/O functions as indicated by the pin name.

The following table lists the recommended pin connections for different configurations of SPO pins if an SPO pin is unused. Note that this table is not applicable to SPO pins which act as AXRES during boot up.

SPO Pin Configuration	Recommended pin connection if unused
CS	Connect to Ground
HI	Leave Open
SH	Leave Open
GPO	Refer to “Unused GPO Pin Connection” Table
BUZ	Leave Open
Disabled	Leave Open

Unused SPO pins which act as AXRES during boot up should be left open and should be disabled through the I2C configurable register map (using Ez-Click or any other configuration tool mentioned in section “Configuring CY8CMBR3xxx” of CY8CMBR3xxx CapSense Design Guide).

The following table lists the recommended pin connections for different drive modes of GPO pins if a GPO pin is unused. Note that this table is not applicable to GPO pins which act as AXRES during boot up.

Open Drain Low	Connect to Ground
Strong	Leave Open

- Dynamically sets all threshold parameters for button sensors, depending on the noise in the environment.
- Can be enabled or disabled through the register map.
- Applicable only to button sensors.
- Mutually exclusive from the EMC feature. If EMC is enabled, automatic threshold is automatically disabled.
- Allows overriding of calculated thresholds with particular values specified through the register map. Refer to the CY8CMBR3xxx CapSense Design Guide for more details.

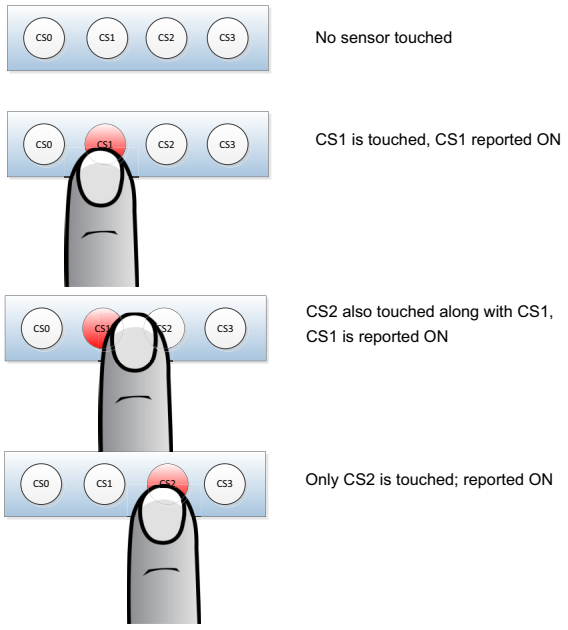
This feature allows specification of the minimum change in sensor capacitance that can trigger a sensor state change (OFF to ON or vice-versa).

- Sensitivity can be specified individually for each CapSense button and slider.
- Sensitivity can be specified as one of the four available values: 0.1 pF, 0.2 pF, 0.3 pF, and 0.4 pF.
- Higher sensitivity values can be used for thick overlays or small button diameters.
- Lower sensitivity values should be used for large buttons or thin overlays to minimize power consumption.

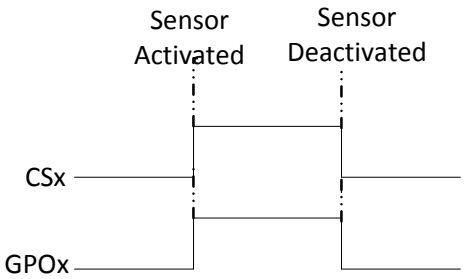
icn-5.8(ues.5.1bem]TJ0 -1.1033 TD 0017 Tc Tw(act)vted .)Tj F1 1 Tf6.96 0

- The CY8CMBR3xxx family features the robust CSD PLUS capacitive sensing algorithm.
- Uses pseudo-random sequence (PRS) clock source to minimize electromagnetic interference.
- Provides advanced noise immunity algorithm, that is, electromagnetic compatibility (EMC), for superior noise immunity against external radiated and conducted noise
  - EMC algorithm has higher average power consumption. For low-power applications, where noise conditions are not extreme, this feature can be disabled using the EZ-Click tool.
- Provides median and IIR filters for button and slider sensors.
- Provides an Advanced-Low-Pass (ALP) filter for proximity sensors.

- Distinguishes between signals from closely spaced buttons, eliminating false touches.
- Can be enabled or disabled individually on each CapSense button.
- On touch detection by two or more sensors on which FSS is enabled, only the first touched sensor reports active status.
- Allows only one button at a time to be in the Touch state.
- Supported only on CapSense buttons.

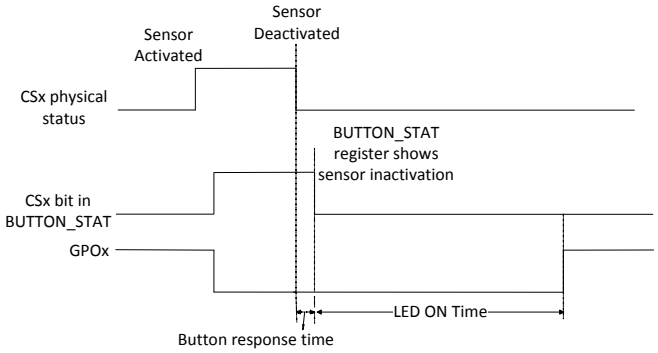


- Supports up to eight GPOs, multiplexed with sensor inputs or other functionality, depending on the part number.
- Provides GPO status control. GPOs can be configured to be controlled by the sensor input or the host through the I^2C interface.
- Allows for configurable Active LOW or Active HIGH logic output. The Active LOW logic output can be configured to directly drive LEDs in the current sink mode. The Active HIGH logic output can be configured to interface the GPOs with the host and other circuits.
- The GPOx status will not be retained in the Deep Sleep mode. The GPOx output state will be reset to default during deep sleep and upon wake-up from deep sleep.



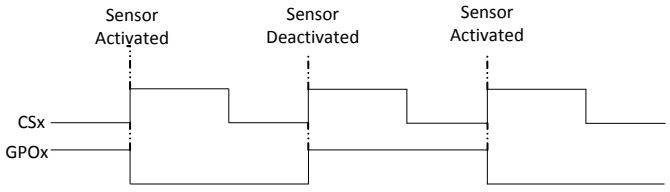
- Supports two drive modes:
  - Open-drain drive mode (HIGH-Z and GND) for analog voltage outputs and LED direct drive
  - Strong drive mode (V_{DD} and GND) to interface with the host and other circuits
- Supports PWM on GPOs for LED brightness control. Two different duty cycles can be configured for Sensor Touch and No Touch states (Active and Inactive state duty cycles). When the GPO is host-controlled, and if the PWM control is enabled for the GPO, the same Touch and No Touch duty cycles will be used for the On and Off states of the host-controlled GPO.
- When the proximity sensor is enabled, the proximity event controls the respective GPOs. A touch event on a proximity sensor is indicated only through the I^2C register map.
- Sensor fault conditions are indicated with the pulse signal on the respective GPOs at power-up by system diagnostics.

- Keeps the GPO status ON for a particular period of time after the falling edge of a sensor, for better visual indication through LEDs



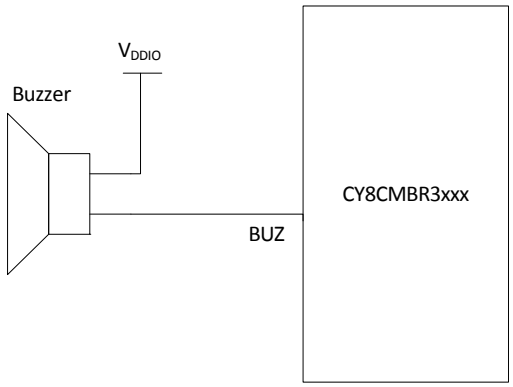
- Can be enabled only when the GPO is directly controlled by a CapSense sensor
- Can be enabled or disabled on each sensor and the ON Time duration can be configured from 0 to 2 seconds in 20-ms increments
- Can be enabled in all configurations of GPOs except the Toggle mode
- Not applicable when the sensor status is turned off by Sensor Auto Reset

- The controller can toggle the GPO state at every rising edge of a sensor activation event to mimic the functionality of a mechanical toggle switch (a touch event for a button sensor and a proximity event for proximity sensors activates a sensor).

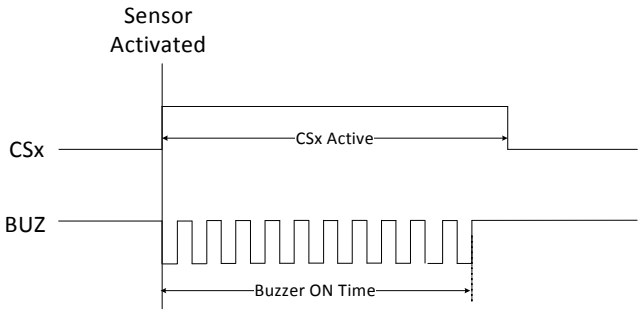


- Can be enabled only when the GPO is directly controlled by a capacitive sensor.
- Can be enabled or disabled individually on each capacitive sensor.
- Can be enabled in all configurations of GPOs—that is, Active LOW and Active HIGH DC output, PWM output, open-drain, and strong drive modes.

- Produces a PWM signal to drive a Piezo-Buzzer that generates audio feedback when a touch is detected on a CapSense button or a guard sensor.
- Supports buzzer connection, as shown in the following figure. [9]

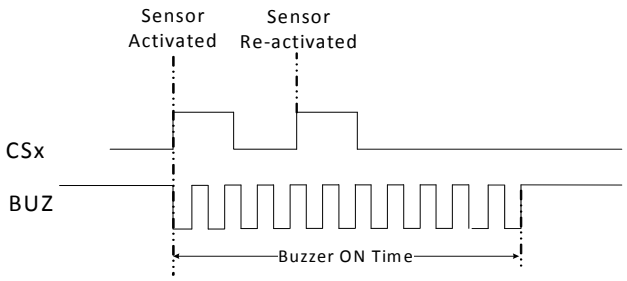


- PWM frequency is configurable: The buzzer frequency is configurable to meet different Piezo-Buzzer drive requirements and to provide different tones. The buzzer frequency may be configured either by using the EZ-Click tool or by writing to the corresponding control register. Refer to System Specifications on page 27 for the supported buzzer frequencies.
- Generates PWM output for a fixed duration (ON time) when a touch is detected. The ON time is configurable through EZ-Click, from 100 ms to 12.7 s, in steps of 100 ms,
- Buzzer signal output and EMC (refer to the CY8CMBR3xxx Registers TRM) are mutually exclusive features. These must not be enabled simultaneously.



The buzzer output does not restart if multiple trigger events occur before the Buzzer ON Time elapses.

9. Buzzer must be connected between V_{DDIO} and the BUZ pin. If V_{DDIO} is not available on the device, connect the buzzer to V_{DD} instead of V_{DDIO}.

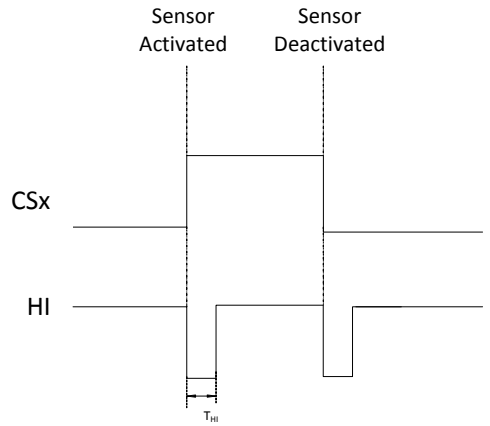


If the buzzer is not currently active, the buzzer output starts on each trigger event.

- When the buzzer is enabled, the buzzer output toggles between a Logic HIGH state and a Logic LOW state, to drive the buzzer when active. When the buzzer is inactive, the buzzer output maintains a Logic HIGH state.
- The buzzer ON Time has a range of (1 to 127) × 100 ms.

This feature generates a pulse signal on any change in the CapSense sensors' status.

- The host interrupt is an active LOW pulse signal generated on the $\overline{HI}$ pin during any change in the sensor status or slider position.
- The duration of the active LOW host interrupt pulse is T_{HI} (refer to System Specifications on page 27).
- The minimum time between two $\overline{HI}$ pulses is equal to one refresh interval.



- The host interrupt pin has the open-drain low-drive mode.
- This pin is powered by V_{DDIO} in CY8CMBR3108. This allows communication with a host processor at voltage levels lower than the chip V_{DD}.
- Only one pin can be configured as the host interrupt on devices that have a host interrupt functionality on multiple pins.

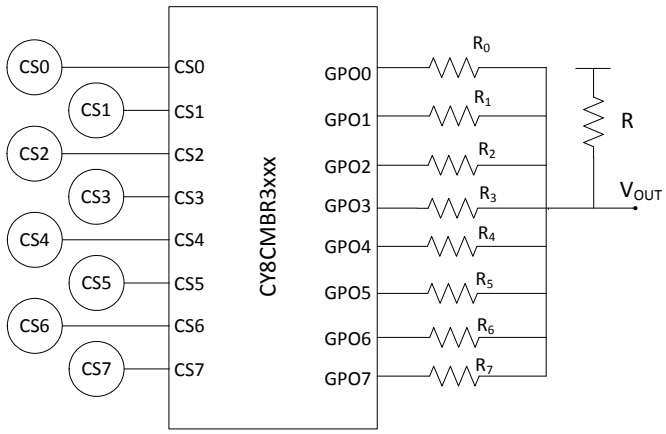
- Allows to read both current status (CS) and latch status (LS) to avoid missing button touches.
- CS and LS can be read through registers, BUTTON_STAT, and LATCHED_BUTTON_STAT respectively.

Table 10 explains the various combinations of CS and LS.

0	0	CSx is not touched during the current I^2C read Host has already acknowledged any previous CSx touch in the previous I^2C read
0	1	CSx was touched before the current I^2C read This CSx touch was missed by the host

Some of the applications use analog voltage as an effective method to indicate the sensor status to the host controller. A simple external resistor network can be used with GPOs of CY8CMBR3xxx to generate analog voltage output upon touch detection for such applications.

The CY8CMBR3xxx GPOs support the open-drain low-drive mode. In this mode, the sensor “touch” state is indicated by a logic LOW signal on the GPO and a "no touch" state is indicated by the HIGH-Z signal. With the external resistor shown in Figure 12, when a sensor is touched, the respective GPO is driven to a logic LOW signal. This forms a simple voltage divider and produces a voltage output. All the other GPOs are in HIGH-Z states because their respective sensors are in the "no touch" state.



The output analog voltage can be calculated based on the following equation:

$$Vout = \frac{\text{VDD x Rn}}{R + Rn}$$

Here, Rn represents the series resistor value of any given GPO.

If more than one button is activated at the same time, the Rn becomes equivalent (parallel) to all Rn resistors.

- For the circuit represented in Figure 12 to work, GPOs should be configured in the Active LOW logic, open-drain drive mode. PWM must be disabled and the CSx-to-GPOx direct drive must be enabled (that is, GPOs must be configured as sensor-controlled).
- The FSS feature can be enabled so only one button is reported ON at a time.

System Diagnostics is a BIST feature that tests for faulty sensor, shield, or CMOD conditions at device resets.

- If any sensor fails these tests, a 50-ms pulse is sent out on the corresponding GPO (that is, the pulse is observed on GPOx if CSx fails the test), and the sensor is disabled.
- If the shield fails the tests, a 50-ms pulse is sent out on all GPOs and all the sensors are disabled.
- If CMOD fails the tests, a 50-ms pulse is sent out on all GPOs and all the sensors are disabled.
- System Diagnostics failure pulses are sent within device boot-up time.
- The System Diagnostics status is also updated in the register map. Therefore, the host can also read test results through the I^2C interface.

If the parasitic capacitance of a sensor is more than 45 pF, the sensor is disabled.

If the value of CMOD is less than 1 nF or greater than 4 nF, all sensors are disabled (the recommended value of CMOD is 2.2 nF).

System Diagnostics also checks for the following errors:

- Sensor shorted to V_{ss}[10]
- Sensor shorted to V_{DD}
- Sensor shorted to another sensor
- Sensor shorted to shield

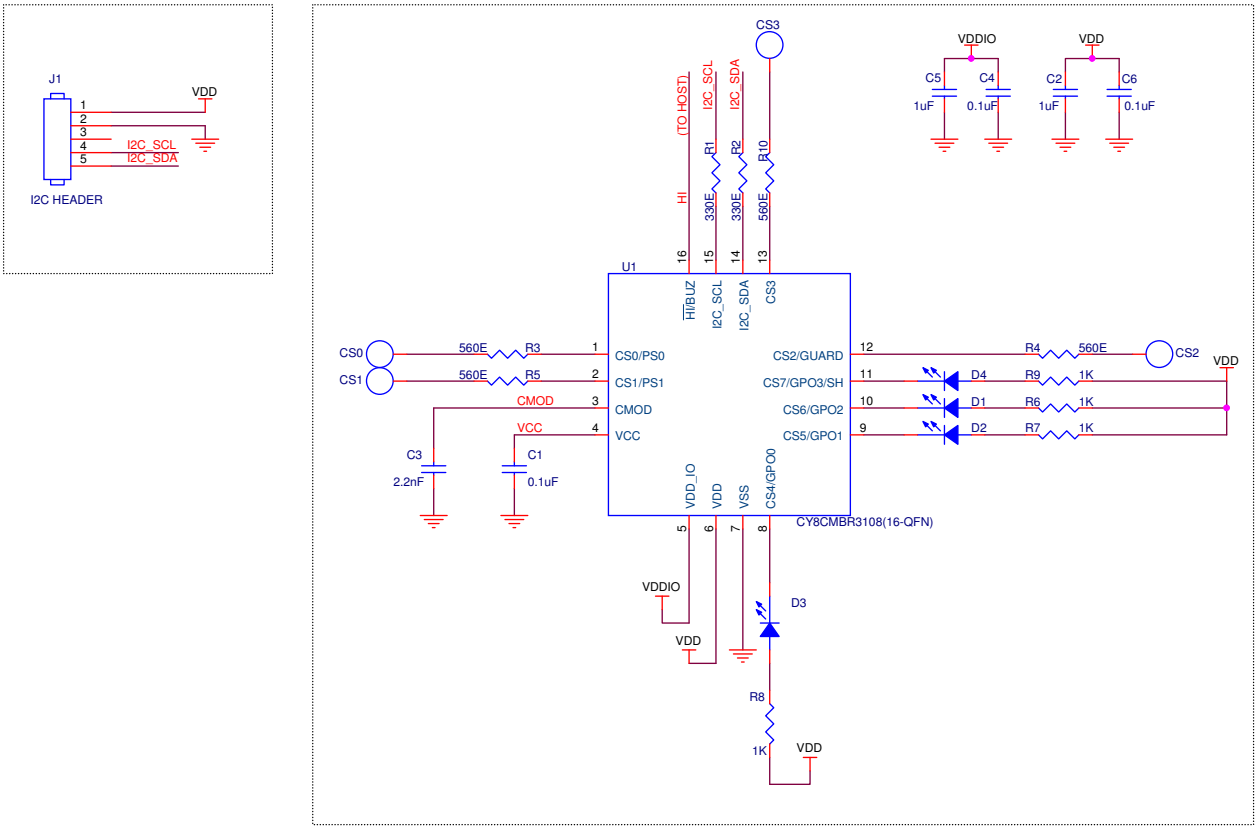
The CY8CMBR3xxx family features an I^2C configurable register map. The CY8CMBR3xxx registers are divided into three categories, as Table 11 shows.

Configuration Registers	0x00-0x7E	These registers contain the configuration data for the CY8CMBR3xxx controllers. A host can write into these registers and save the data to non-volatile memory by writing to CTRL_CMD command register. Note that the new configuration takes effect only after the configuration is saved to non-volatile memory and the device is reset (see CY8CMBR3xxx Resets on page 31).
Command Registers	0x80-0x87	These registers accept commands from host. Any command written to these register is executed within $T_{I2C_LATENCY_MAX}$ from the I^2C acknowledgement of the command.
Status Registers	0x88-0xFB	These are read only registers and indicate the status of command execution, system diagnostics and sensor data.

The CY8CMBR3xxx devices feature a safe register map update mechanism to overcome configuration data corruption, which can occur due to power failure during execution of "Save" command or any other spurious events.

If the configuration data is corrupted when the device is saving data, on the next reset, the devices reconfigure themselves to the last known valid configuration. If there is no valid configuration saved by user, the devices load the factory default configuration as specified in Register TRM.

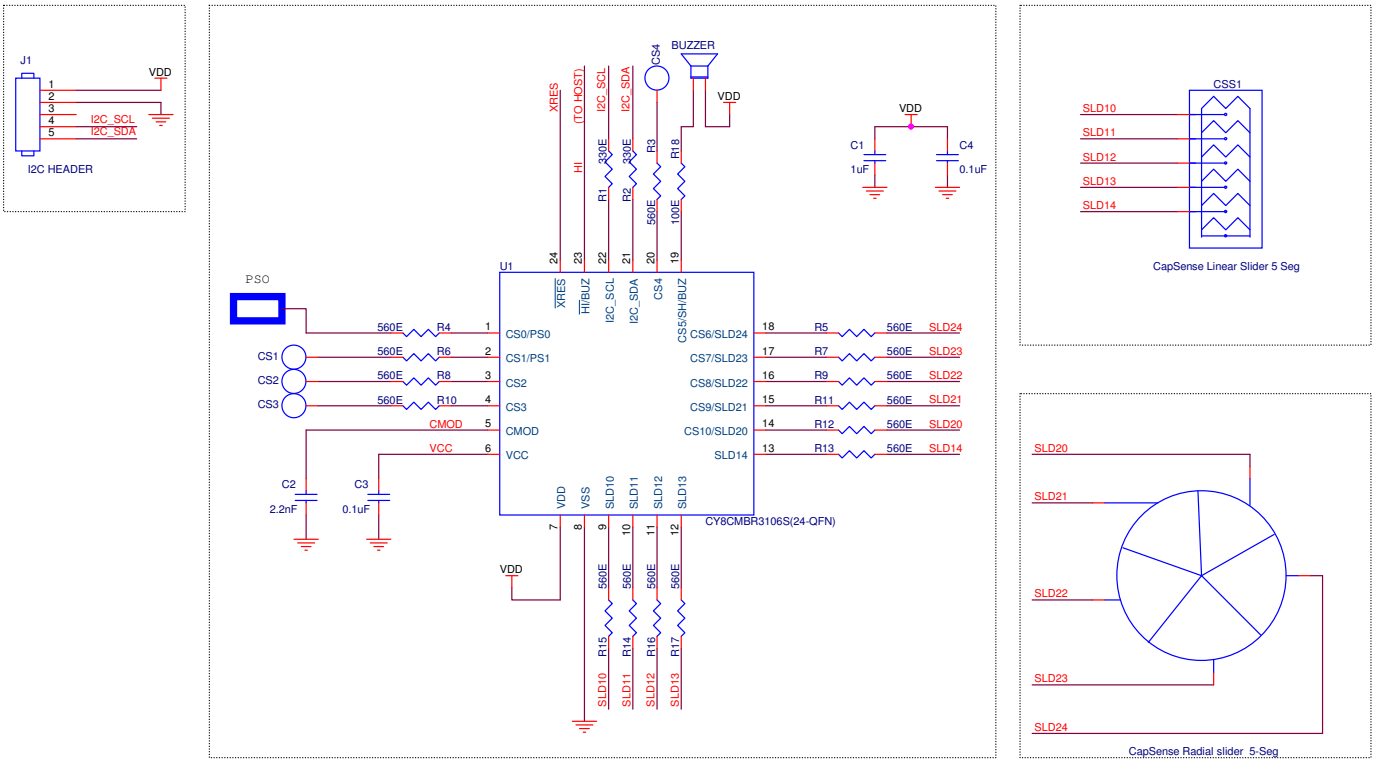
10. Sensor shorts to Vss are detected for all pins other than the pin, which is $\overline{\text{AXRES}}$ also for a given package.



In Figure 13[11, 12], the CY8CMBR3108 device is configured in the following manner:

- CS0–CS3: CapSense buttons
  - All CapSense pins must have a 560-ohm series resistance (placed close to the chip) for improved noise immunity.
- GPO0–GPO3: To external LEDs
  - LEDs are connected in sinking mode because the CY8MBR3xxx devices have high sink current capability.
  - Series resistances are connected to limit the GPO current to be with I_{IL} limits.
- CMOD pin: 2.2 nF to ground
- VCC pin: 0.1 µF to ground
- VDD pin: To external supply voltage
  - 1-µF and 0.1-µF decoupling capacitors connected to VDD
- VDDIO pin: To supply voltage, which is ≤ VDD
  - VDDIO powers I^2C and $\overline{HI}$ lines.
  - 1-µF and 0.1-µF decoupling capacitors connected to VDDIO.
- I2C_SCL and I2C_SDA pins: 330 ohms to the I^2C header
  - For I^2C communication: It is assumed that the I^2C line pull-up resistors are present on the host side outside the I^2C header.
- $\overline{HI}$ pin: To host
  - To prompt the host to initiate an I^2C transaction for reading the changed sensor status.

11. VCC should be connected to VDD for 1.71 V ≤ VDD ≤ 1.89 V.
12. Proper ground layout is important for better SNR performance. Refer to the CY8CMBR3xxx CapSense Design Guide and Getting started with CapSense guide for all layout guidelines.



In Figure 14[13, 15], the CY8CMBR3106S device is configured in the following manner:

- PS0: CapSense proximity sensor
- CS1–CS4: CapSense buttons[14]
- CMOD pin: 2.2 nF to ground
- VCC pin: 0.1 uF to ground
- VDD pin: To external supply voltage
  - 1-µF and 0.1-µF decoupling capacitors connected to VDD
- SLD10-SLD14: CapSense linear slider segments
- SLD20-SLD24: CapSense radial slider segments
- BUZ: To buzzer
  - AC buzzer (1-pin).
  - Buzzer second pin to ground.
- I2C_SCL and I2C_SDA pins: 330 ohm to the I^2C header. It is assumed that the I^2C line pull-up resistors are present on the host side outside the I^2C header.
  - For I2C communication.
- $\overline{HI}$ pin: To host
  - To prompt the host to initiate an I^2C transaction for reading the changed sensor status.
- $\overline{XRES}$ pin: Floating
  - For external reset.

13. VCC should be shorted to VDD for 1.71 V ≤ VDD ≤ 1.89 V.
14. All CapSense pins have 560-ohm series resistance (placed close to the chip) for improved noise immunity.
15. Proper ground layout is important for better SNR performance. Refer to the CY8CMBR3xxx CapSense Design Guide and Getting started with CapSense guide for all layout guidelines.

The CY8CMBR3xxx family of controllers contains three supply domains: V_{DD}, V_{CC}, and V_{DDIO}.

- V_{DD}: This is the primary supply to the chip and can be powered from 1.8 V ± 5% (Externally regulated mode) or 1.8 to 5.5 V (Internally regulated mode). The CapSense controller is powered by the V_{DD} supply, and all the I/O signal levels (except I^2C lines, $\overline{HI}$, and $\overline{XRES}$) are referenced with respect to the V_{DD} supply. For packages and MPNs that do not have V_{DDIO}, the I^2C SDA, I^2C SCL, $\overline{HI}$, and $\overline{XRES}$ signal levels are also referenced with respect to the V_{DD} supply.
- V_{DDIO}: This is the supply input for I^2C SDA, I^2C SCL, $\overline{HI}$, and $\overline{XRES}$ lines. The signal levels of these I/Os are referenced with respect to V_{DDIO}. The V_{DDIO} supply can be as low as 1.71 V and as high as the voltage of the V_{DD} supply. The V_{DDIO} should not be powered at a voltage higher than that of the V_{DD} supply. The V_{DDIO} is available only on select packages. For a package that does not have V_{DDIO}, the I^2C SDA, I^2C SCL, $\overline{HI}$, and $\overline{XRES}$ signal levels are referenced with respect to the V_{DD} supply.
- V_{CC}: This is the internal regulator output, which powers the core and capacitive sensing circuits. A 0.1-µF, 5-V ceramic capacitor should be connected close to the V_{CC} pin for better performance.
- Power sequencing: The CY8CMBR3xxx device does not require any power supply sequencing for the VDD and VDDIO supplies. Either of these supplies can ramp earlier or later than the other. The only requirement is that VDDIO should not be greater than VDD.
- 1.8-V externally regulated operation: When V_{DD} is powered with a 1.8 V ±5% supply, the V_{CC} and V_{DD} pins should be shorted externally and the SUPPLY_LOW_POWER bit in the DEVICE_CFG3 register should be set to 1 through the I^2C interface (refer to the CY8CMBR3xxx Registers TRM for details on the register). When the VCC and VDD pins are shorted, this bypasses the internal voltage regulator. Under this condition, make certain that VDD does not exceed 1.89 V.

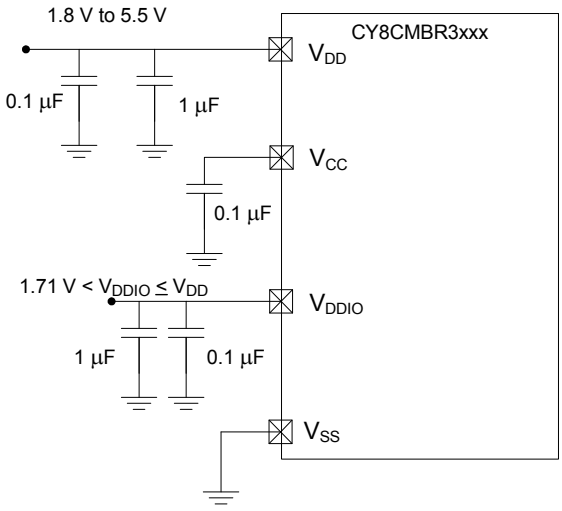
If EZ-Click is used to configure the device, it automatically takes care of the required register settings based on the voltage settings selected in EZ-Click.

The CY8CMBR3xxx family of controllers is factory-configured for 1.8-V to 5.5-V operation. To configure a factory-configured device for 1.8-V externally regulated operation, you can use the following procedure:

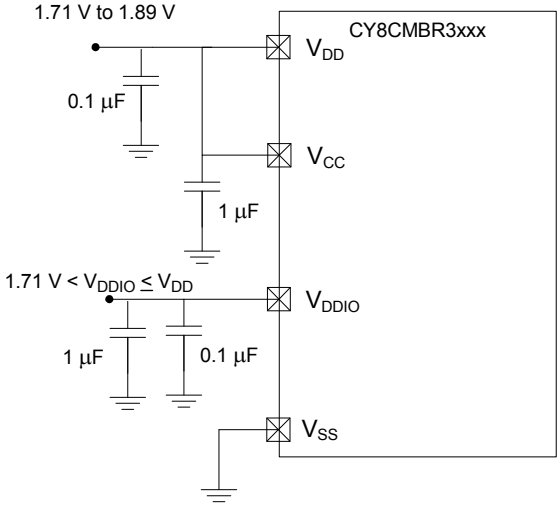
- Short V_{DD} and V_{CC}.
- Power the device at 1.8 V (note that regardless of the value of the SUPPLY_LOW_POWER bit, the device can be powered at 1.8 V for configuring the device; only CapSense operation is not guaranteed if the SUPPLY_LOW_POWER bit is not properly configured)
- Use EZ-Click to configure the device for 1.8-V operation.
- Save and reset the device.
- Ground consideration: Both the V_{SS} pin and the metal pad (E-pad) of the device should be connected to board ground.

[16]

Power supply connections when $1.8 \le V_{DD} \le 5.5$ V



Power supply connections* when $1.71 \le V_{DD} \le 1.89$ V



*SUPPLY_LOW_POWER bit in DEVICE_CFG3 register should be set to 1 to operate device at 1.8V (±5%)

16. Proper ground layout is important for best performance. Refer to the layout guidelines mentioned in the CY8CMBR3xxx CapSense Design Guide and Getting started with CapSense guide.

[17]

V_{DD_MAX}	Max voltage on the V_{DD} pin relative to V_{SS}	–40 °C to +85 °C T_A, absolute maximum	–0.5	–	6	V
V_{DDIO_MAX}	Max voltage on the V_{DDIO} pin relative to V_{SS}	–40 °C to +85 °C T_A, absolute maximum	0.5	–	6	V
V_{CC_MAX}	Max voltage on the VCC pin relative to V_{SS}	Absolute maximum	–0.5	–	1.89	V
V_{IO}	DC input voltage relative to V_{SS} on I/O	–40 °C to +85 °C T_A, absolute maximum	–0.5	–	V_{DD}+0.5	V
ESD_HBM	Electrostatic discharge, human body model	Human body model ESD.	2200	–	–	V
ESD_CDM	Electrostatic discharge, charged device model	Charged device model ESD	500	–	–	V
I_{LU}	Latch-up current limits	Maximum/minimum current to any input or output, pin-to-pin or pin-to-supply	–140	–	140	mA
I_{IO}	Current per GPIO		–	–	25	mA

T_O	Operation temperature	Ambient temperature inside system enclosure	–40	25	85	°C
T_J	Junction temperature		–40	–	100	°C

DC Chip-Level Specifications

The specifications in Table 14 are valid under these conditions: –40 °C ≤ T_A ≤ 85 °C. Typical values are specified at T_A = 25 °C, V_{DD} = 3.3 V, and are for design guidance only.

V_{DD}	Chip supply voltage	V_{CC} shorted to V_{DD}	1.71	1.8	1.89	V
		V_{CC} not shorted to V_{DD}. V_{CC} connected to 0.1 µF decoupling capacitor	1.8	–	5.5	V
V_{DDIO}	Supply voltage I/O	1.71 V < V_{DD} < 1.89 V	1.71	–	V_{DD}	V
		1.8 V < V_{DD} < 5.5 V	1.71	–	V_{DD}	V
V_{DD_RIPPLE}	Maximum allowed ripple on power supply, DC to 10 MHz	+25 °C T_A, V_{DD} > 2 V, sensitivity ≥ 0.1 pF	–	–	±50	mV
		+25 °C T_A, V_{DD} > 1.75 V, C_P < 20 pF, sensitivity = 0.4 pF	–	–	±25	mV
C_{EFC}	External regulator voltage bypass (capacitor to be connected to the V_{CC} pin)	X5R ceramic ±10% or better	–	0.1	–	µF
C_{EXC}	Power supply decoupling capacitor on V_{DD}	X5R ceramic or better	–	1	–	µF

17. Usage above the absolute maximum conditions listed in Table 12 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions, but above normal operating conditions, the device may not operate to specification.

XRES DC Specifications

V_{IH_XRES}	Input voltage high threshold on XRES pin	CMOS input	0.7*V_{DD}	–	–	V
V_{IL_XRES}	Input voltage low threshold on XRES pin	CMOS input	–	–	0.3*V_{DD}	V
C_{IN_XRES}	Input capacitance on XRES pin		–	–	7	pF
$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	V_{DD} ≤ 4.5 V	–	0.05*V_{DD}	–	mV
		V_{DD} > 4.5 V	200	–	–	mV

DC I/O Port Specifications

The specifications in Table 16 are valid at –40 °C ≤ T_A ≤ +85 °C. Typical parameters are specified at T_A = 25 °C and are for design guidance only.

V_{OH}	Output voltage HIGH level	I_{OH} = –4 mA at 3 V V_{DD}	V_{DD}–0.6	–	–	V
		I_{OH} = –1 mA at 1.8 V V_{DD}	V_{DD}–0.5	–	–	V
V_{OL}	Output voltage LOW level	I_{OL} = 4 mA at 1.8 V V_{DD}	–	–	0.6	V
		I_{OL} = 10 mA at 3 V V_{DD}	–	–	0.6	V
C_{PIN}	Pin capacitance	All V_{DD}, all packages, all I/Os	–	3	7	pF
I_{TOT_GPIO}	Maximum total sink chip current		–	–	85	mA
R_{PU}	Pull-up resistor	+25 °C T_A, All V_{DD}	3.5	5.6	8.5	kΩ

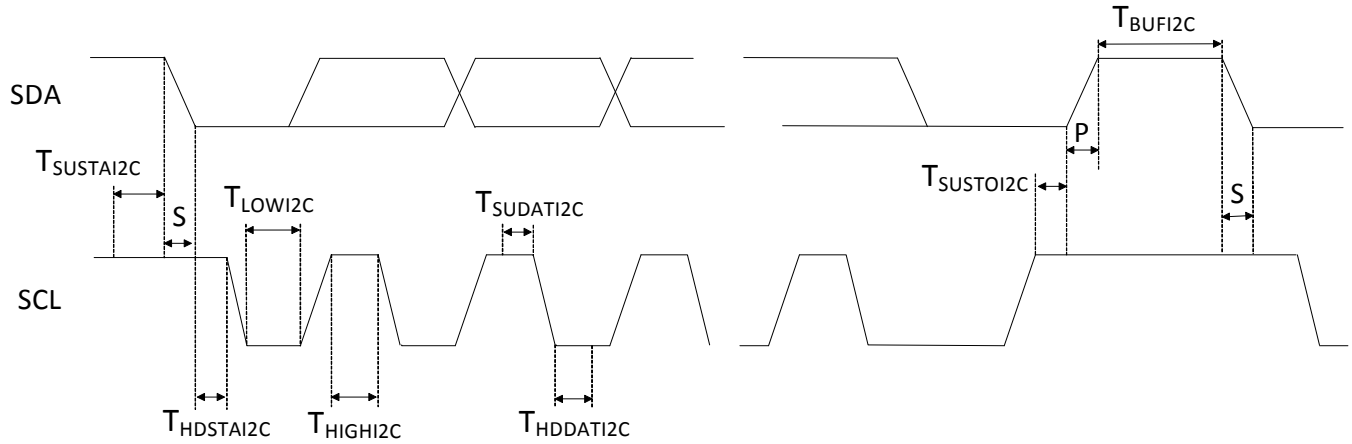
$T_{SR_POWER_UP}$	Power supply slew rate during power-up	–40 °C ≤ TA ≤ 85 °C, all V_{DD}	1	–	67	V/ms

XRES AC Specifications

T_{XRES}	External reset pulse width	–40 °C ≤ T_A ≤ 85 °C, all V_{DD}	5	–	–	µs

18. V_{IH} must not exceed V_{DD} + 0.2 V.

FSCLI2C_FM	I^2C SCL clock frequency		0	–	400	kHz
THDSTAI2C_FM	Hold time (repeated) START condition; after this period, the first clock pulse is generated		0.6	–	–	µs
TSUSTAI2C_FM	Setup time for a repeated START condition		0.6	–	–	µs
TLOWI2C_FM	LOW period of the SCL clock		1.3	–	–	µs
THIGHI2C_FM	HIGH period of the SCL clock		0.6	–	–	µs
THDDATI2C	Data hold time		0	–	–	µs
TSUDATI2C_FM	Data setup time		100	–	–	ns
TSUSTOI2C_FM	Setup time for I^2C STOP condition		0.6	–	–	µs
CB_FM	Capacitive load for each I^2C bus line		–	–	400	pF
TVDDATI2C_FM	Data valid time		–	–	0.9	µs
TVDACKI2C_FM	Data valid acknowledge time		–	–	0.9	µs
TSPI2C_FM	Pulse width of spikes suppressed by the input filter		–	–	50	ns
TBUFI2C_FM	Bus-free time between STOP and START condition		1.3	–	–	µs
VIL_I2C	Input LOW voltage	2-mA sink	–0.5	–	0.3 * V_{DD}	V
VIH_I2C	Input HIGH Voltage	3-mA sink	0.7* V_{DD}	–	–	V
VOL_I2C_L	Output LOW voltage, low supply range	V_{DD} < 2 V, 3-mA sink	–	–	0.2 * V_{DD}	V
VOL_I2C_H	Output LOW voltage, high supply range	V_{DD} > 2 V, 3-mA sink	–	–	0.4	V
IOL_I2C_FM	I^2C output low current	Fast Mode, 1.71 V ≤ V_{DD} ≤ 5.5 V, load = CB_SM, V_{OL} = 0.6 V	6	–	–	mA
I2C_VHYS_HV	I^2C input hysteresis	Fast and standard mode I2C speeds. 2 V ≤ V_{DD} ≤ 4.5 V	0.05 * V_{DD}	–	–	mV
I2C_VHYS_5V5	I^2C input hysteresis	Fast and standard mode I2C speeds. 4.5 V < V_{DD} < 5.5 V	200	–	–	mV
I2C_VHYS_LV	I^2C input hysteresis	Fast and standard mode I2C speeds. V_{DD} < 2 V	0.1 * V_{DD}	–	–	mV



The specifications in the following table are valid at T_A = 25 °C and V_{DD} = 5 V, unless otherwise specified.

C_P	Supported parasitic capacitance range of sensors	0.2-pF sensitivity, SNR 5:1	5	–	45	pF
		0.1-pF sensitivity, SNR 5:1	12	–	35	pF
		0.1-pF sensitivity, SNR 4:1	5	–	45	pF
C_{MOD}	Value for C_{MOD} external capacitor	5-V rating, X7R or NP0 Cap. $C_P \le 45$ pF	–	2.2	–	nF
I_{AVG_NT}	Average current per button with no finger touch	V_{DD} = 5 V, 3.3 V, 2.5 V, 1.8 V, C_P = 10 pF, 2 buttons, Refresh interval = 120 ms, EMC disabled, 0.4-pF sensitivity	–	–	22	µA
I_{AVG_WT}	Average current with finger touch	V_{DD} = 5 V, 3.3 V, 2.5 V, 1.8 V, C_P = 10 pF, 8 buttons, Refresh interval =120 ms, EMC disabled, 0.4-pF sensitivity	–	–	600	µA
I_{AVG_WF}	Average current with EMC	V_{DD} = 5 V, 3.3 V, 2.5 V, 1.8 V, C_P = 10 pF, 8 buttons, Refresh interval =120 ms, EMC enabled, 0.4-pF sensitivity	–	–	300	µA
I_{AVG_NF}	Average current without EMC	V_{DD} = 5 V, 3.3 V, 2.5 V, 1.8 V, C_P = 10 pF, 8 buttons, Refresh interval = 120 ms, EMC disabled	–	–	100	µA
I_{DS}	Deep Sleep current with I^2C on	$V_{DD} \le 3.3$ V, T_A = 25 °C, I^2C Enabled	–	2.5	–	µA
T_{BOOT_SYS}	Boot-up time (time from power-up to first sensor scan) with system diagnostics enabled and EMC disabled	16 buttons, $C_P \le 18$ pF	–	–	900	ms
T_{BOOT_WF}	Boot-up time (time from power-up to first sensor scan) with no system diagnostics and EMC enabled	10 buttons, $C_P \le 18$ pF	–	–	850	ms
T_{BOOT}	Boot-up time (time from power-up to first sensor scan) with no system diagnostics and EMC disabled	16 buttons, $C_P \le 18$ pF	–	–	400	ms
$T_{BOOT_SYS_WF}$	Boot-up time (time from power-up to first sensor scan) with both system diagnostics and EMC enabled.	10 buttons, $C_P \le 18$ pF	–	–	1350	ms
$T_{I2CBOOT}$	Boot up time (time from power to I^2C ready)		–	–	15	ms
$T_{I2C_LATENCY_MAX}$	Time between I^2C command and execution (for all commands except the "Save"[19] command)		–	–	50	ms

19. Save command takes 220 ms to execute.

(continued)

T_{HI}	Host interrupt pulse width	5 V, 1.8 V	200	–	700	µs
F_{BUZ_4}	Buzzer output frequency	5 V, 1.8 V	–	4.00	–	kHz
$F_{BUZ_2.67}$	Buzzer output frequency	5 V, 1.8 V	–	2.67	–	kHz
F_{BUZ_2}	Buzzer output frequency	5 V, 1.8 V	–	2.00	–	kHz
$F_{BUZ_1.60}$	Buzzer output frequency	5 V, 1.8 V	–	1.60	–	kHz
$F_{BUZ_1.33}$	Buzzer output frequency	5 V, 1.8 V	–	1.33	–	kHz
$F_{BUZ_1.143}$	Buzzer output frequency	5 V, 1.8 V	–	1.14	–	kHz
F_{BUZ_1}	Buzzer output frequency	5 V, 1.8 V	–	1.00	–	kHz
F_{PWM}	GPO PWM frequency	5 V, 1.8 V	–	106.7	–	Hz
T_{SNS_RST5}	Sensor auto-reset interval 5 sec	5 V, 1.8 V	–	5	–	sec
T_{SNS_RST20}	Sensor auto-reset interval 20 sec	5 V, 1.8 V	–	20	–	sec
$T_{FAULTY_SNS_PULSE}$	Pulse width on GPOx when the corresponding CSx fails the system diagnostics test		–	50	–	ms
C_{P_SHIELD}	Maximum C_P supported for shield electrode		–	–	100	pF

The CY8CMBR3xxx family of controllers is designed with multiple low-power operational states to meet the low-power requirements of battery-powered applications. These controllers have the following operational states (see Figure 17):

1. Boot: The devices load the last-known configuration data and run system diagnostics tests.
2. Active: The sensors are scanned at a fixed refresh rate to determine the presence of touch, proximity, or finger position on a slider, and any configured outputs (GPOs, buzzer and HI) are driven. The refresh time in this state is the total scanning and processing time of sensors, or 20 ms (typical) whichever is higher.
3. Look-for-Touch: All the sensors are scanned at a much slower, user-configured refresh interval, and any enabled GPOs (such as PWM or DC Toggle) are driven.
4. Look-for-Proximity: Only proximity sensors enabled for wake-on approach are scanned. No outputs are driven in this state.
5. Deep Sleep: No sensors are scanned, and the CY8CMBR3xxx devices are in a Low-power State with no processing. The GPO status is reset to the default value in the Deep Sleep mode.
6. Configuration: No scanning or reporting occurs and the devices wait for a reset for the configuration settings to take effect.

The CY8CMBR3xxx controllers automatically manage transitions between four operational states (Boot, Active, Look-for-Touch, and Look-for-Proximity). The host can force transition in and out of the Deep Sleep state. A host command can alter the configuration data, causing a transition to the Configuration state. A transition to Configuration state can also occur automatically after boot, if the configuration data is corrupted.

The Active state emphasizes a high refresh rate (that is, low refresh interval) for fast responses to button touches and proximity events. The Look-for-Touch state enables low power consumption during periods of no-touch activity.

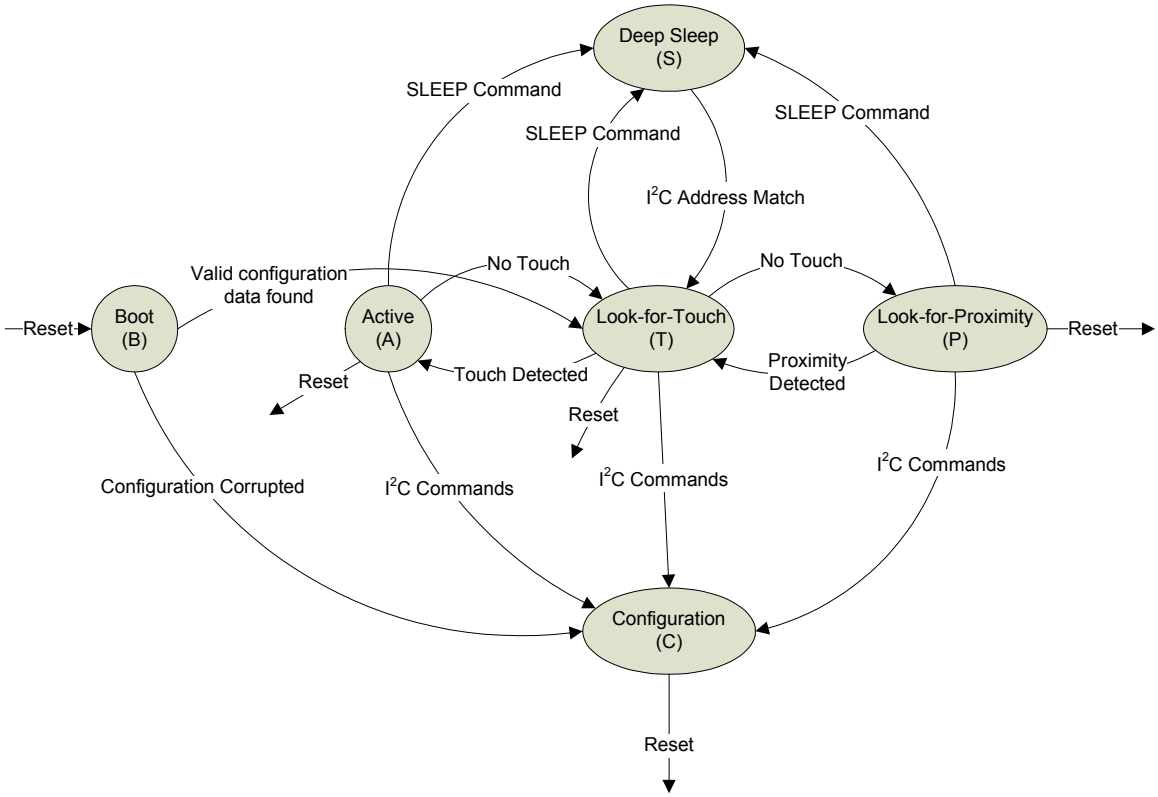
The Look-for-Proximity state allows ultra-low power consumption when a human body is not in close proximity. This state is entered only if the wake-on-approach feature is enabled (and the toggle is disabled). In this state, the CY8CMBR3xxx controllers periodically scan proximity sensors to determine the presence of a human body. If they detect human presence, the controllers enter the Look-for-Touch state, in which they scan all sensors at a slow, user-configured refresh interval. If a touch is detected, the controllers enter the Active state. The controllers remain in the Active state as long as the touch is present. In this state, they update the sensor status and drive the corresponding outputs. A transition from Active to Look-for-Touch occurs when no touch is detected and the buzzer is not driven. Similarly, a transition from Look-for-Touch to Look-for-Proximity occurs when no proximity is detected.

The following parameters configure the operational states:

- State timeout (Register STATE_TIMEOUT) defines the following:
  - Minimum time (in seconds) of no touch activity in the Active state
  - Minimum time to trigger a transition to the Look-for-Touch state
  - Minimum time of no touch activity in the Look-for-Touch state
  - Minimum time to trigger a transition to the Look-for-Proximity state
- Refresh Interval (Register REFRESH_CTRL) defines the minimum time between the start of subsequent scans in the Look for Touch and Look-for-Proximity states.
- The Refresh Interval for the Active state is fixed at 20 ms.

During all three operational states—Active, Look-for-Touch, and Look-for-Proximity, within each refresh interval, the devices enter a Low-power State after scanning and processing the requisite sensors. This helps to maintain the lowest average power consumption within any refresh interval. Note that if any I^2C traffic is detected on the I^2C bus or the I2C_SCL is held low, the devices do not enter the Low-power State after scanning and processing the sensors. This ensures that the devices do not send unnecessary NACKs to I^2C transactions because of periodical entry to the Low-power State. Therefore, the device requires I^2C interface to be in “free” state and I^2C lines to be pulled up for power optimization.

Refer to section “System Design Recommendations for Low Power Consumption” in CY8CMBR3xxx CapSense Design Guide for low power design considerations.


Deep Sleep
(S)
SLEEP Command
SLEEP Command
SLEEP Command
I2C Address Match
Valid configuration
data found
No Touch
No Touch
Reset
Boot
(B)
Active
(A)
Look-for-Touch
(T)
Look-for-Proximity
(P)
Reset
Reset
Touch Detected
Proximity
Detected
Reset
Configuration Corrupted
I2C Commands
I2C Commands
I2C Commands
Configuration
(C)
Reset

Response time for button and proximity sensors is the minimum amount of time for which the sensor must be active/inactive (touched or proximity present), for the device to detect it as a valid activation or deactivation event.

For the CY8CMBR3xxx device family, response time numbers for different sensors can be estimated using the design toolbox. The following response time numbers are provided in the toolbox:

- R_{FBT}: This value represents the response time for first button touch when the device is in the Look-for-Touch or Look-for-Proximity operational states.
- R_{CBT}: This value represents the response time for consecutive button touches when the device is in the Active operational state.
- R_{FST}: This value represents the response time for the first slider touch when the device is in the Look-for-touch operational state.
- R_{CST}: This value represents the response time for consecutive slider touches when the device is in the Active operational state.
- R_{BSR}: This value represents the response time for button and slider release events when the device is in the Active operational state.
- RProx: This value represents the response time for detecting valid proximity events on a proximity sensor.
- RProx_release: This value represents the response time for proximity release events on a proximity sensor.

The CY8CMBR3xxx family of CapSense controllers has three reset options – two hardware resets and one software reset.

- Hardware Resets
  - Power reset –Toggling the power on the V_{DD} pin of the CapSense controller resets the controller.
  - $\overline{\text{XRES}}$ reset – Pull the device $\overline{\text{XRES}}$ pin LOW for T_{XRES} duration and then pull it HIGH.
- Software Reset

To reset the software, write one SW_RESET command to the command register. All three resets are functionally equivalent, and the CapSense controllers enter the Boot state (refer to the Power Consumption and Operational States section) after any reset.

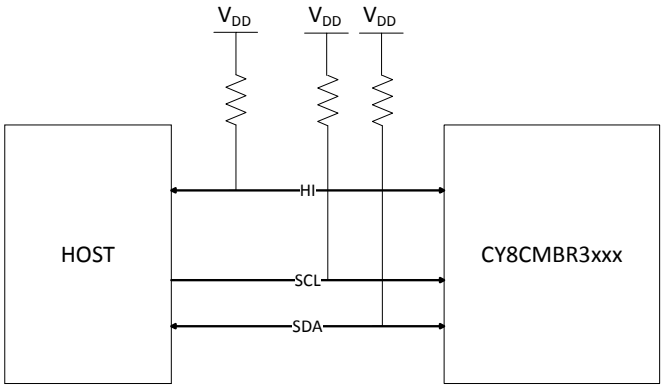
The CY8CMBR3xxx CapSense controllers communicate to the host through the I^2C interface. I^2C is a simple two-wire synchronous communication protocol that uses the following two lines:

- Serial Clock (SCL) –This line is used to synchronize the slave with the master.
- Serial Data (SDA) – This line is used to send data between the master and the slave.

The CY8CMBR3xxx I^2C interface has the following features:

- Bit rate of 400 kbps
- Configurable I^2C slave address (7-bit)
- No bus-stalling or clock-stretching during transactions
- Register-based access to the I^2C master for reads and writes
- Repeated START support

The CY8CMBR3xxx CapSense controllers can be part of a single-slave or a multi-slave environment.



To identify each device on the I^2C bus, a unique 7-bit I^2C slave address is used. When the master wants to communicate with a slave on the bus, it sends a START condition followed by the appropriate I^2C address. The START condition alerts all slaves on the bus when a new transaction starts. The slave with the specified I^2C address acknowledges the master. All the other slaves ignore further traffic on the bus until the next START condition is detected.

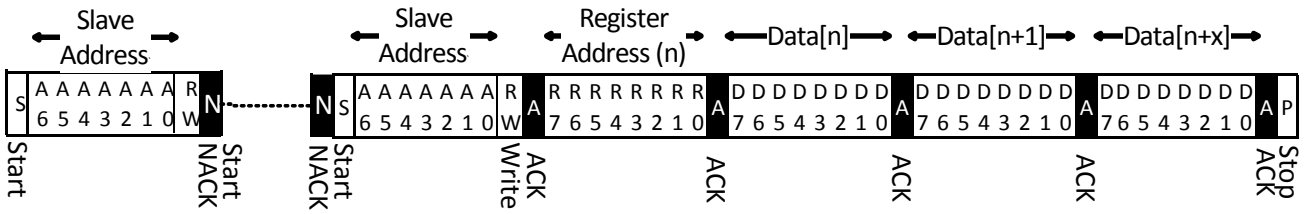
The 7-bit I2C Slave Address for CY8CMBR3xxx devices can be configured by modifying the contents of I2C_ADDR register mentioned in CY8CMBR3xxx Registers TRM. Refer to section “Configuring CY8CMBR3xxx” in CY8CMBR3xxx CapSense Design Guide for more details on how to configure CY8CMBR3xxx registers.

The I2C address can be configured to any value between 0x08 to 0x77. The default I2C address for all CY8CMBR3xxx devices is 0x37.

1. After device reset, the host should wait for $T_{I2CBOOT}$ time before initiating any I^2C communication. The CY8CMBR3xxx CapSense controller family will generate a NACK if the host tries to communicate before this period.
2. The CY8CMBR3xxx controller is expected to NACK the address match event if it is in the low-power state (during any of the operational states – Deep Sleep, Look-for-Touch, Look-for-Proximity, or Active). The controller wakes up from the low-power state on an address match but sends NACK until it transitions into the Active state and, on for the first transaction, in the active state. When the device NACKs a transaction the host is expected to retry the transaction until it receives an ACK.
3. If there is a delay of more than 340 ms between two subsequent bytes within an I^2C transaction, the device may go into low-power state and the host may get a NACK.
4. When the host sends the SAVE_CHECK_CRC command, the device will send a NACK on any subsequent I^2C transactions until the command execution is completed. The time taken to complete the SAVE_CHECK_CRC command is 220 ms typ.
5. The host must not write to read-only registers. All write operations directed to such read-only registers are ignored.

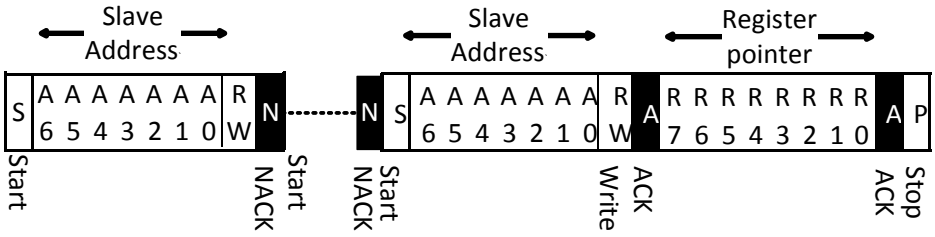
A host performs the following steps during a write operation:

1. The host sends the START condition.
2. The host specifies the slave address, followed by the read/write bit to specify a write operation.
3. The device may NACK the host.
4. The host sends a Repeat Start (or a stop followed by a start condition), followed by the address and read/write bit, to specify a write operation. The host keeps sending the Repeat Start with the address and read/write bits until the device sends an ACK. The device ACKs the host.
5. The host specifies the register address to which it has to write.
6. The device ACKs the host.
7. The host starts sending the data to the device, which is written to the register address specified by the host. This is followed by an ACK from the device.
8. If the write operation includes more bytes, each one is written to the successive register address. Each successive byte is followed by an ACK from the device.
9. After the write operation is complete, the host sends the STOP condition to the device. This marks the end of the communication (see Figure 19).



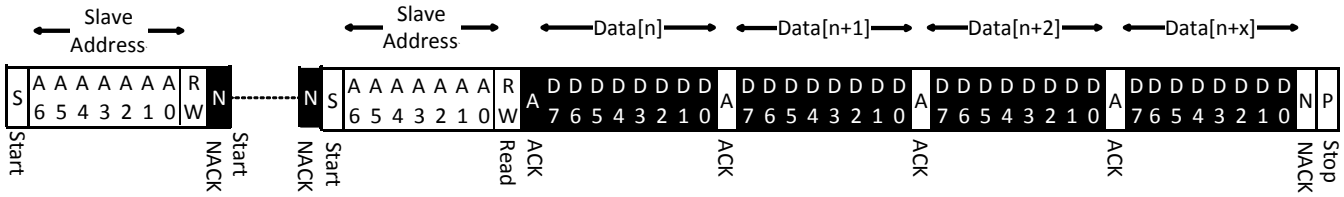
The host sets the device data pointer to specify the starting point for future read operations. Setting the device data pointer involves the following steps:

1. The host sends the START condition.
2. The host specifies the slave address, followed by the read/write bit to specify a write operation.
3. The device may NACK the host.
4. The host sends a Repeat Start, followed by the address and read/write bit, to specify a write operation. The host keeps sending the repeat start with the address and read/write bit until the device sends an ACK.
5. The device ACKs the host.
6. The host specifies the register address. Any further read operation will take place from this address.
7. The host sends the STOP condition (see Figure 20).



The host performs the following steps for a read operation:

1. The host sends the START condition.
2. The host specifies the slave address, followed by the read/write bit to specify a write operation.
3. The device may NACK the host.
4. The host sends a repeat start followed by the address and read/write bit to specify a write operation. The host keeps sending the repeat start with the address and read/write bits until the device sends an ACK.
5. The device ACKs the host.
6. The device retrieves the byte from the pre-specified register address and sends it to the host. The host ACKs the device.
7. Each successive byte is retrieved from the successive register address and sent to the host, followed by ACKs from the host.
8. After the host receives the required bytes, it NACKs the device.
9. The host sends the STOP condition to the device. This marks the end of the communication (see Figure 21).



Legend:

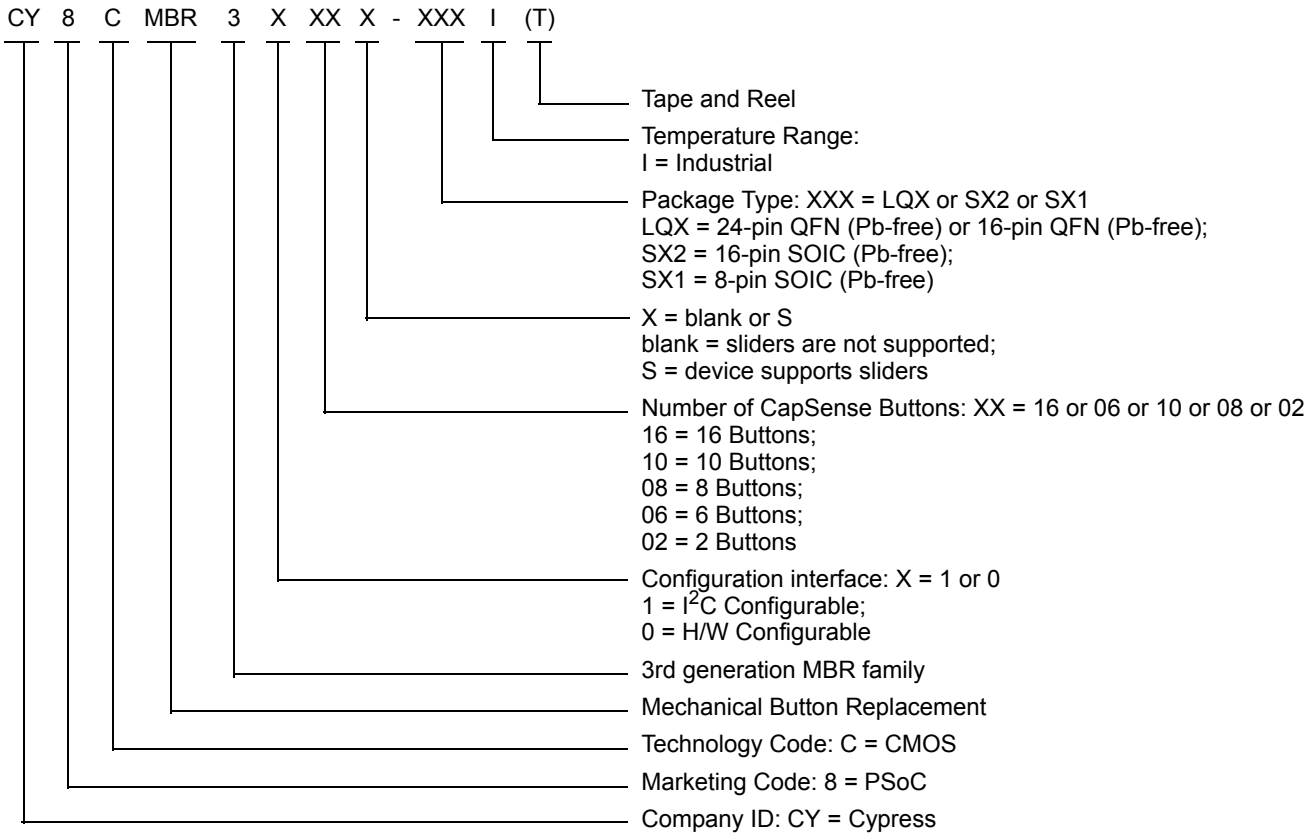
CY8CMBR3xxx to Host

HOST to CY8CMBR3xxx

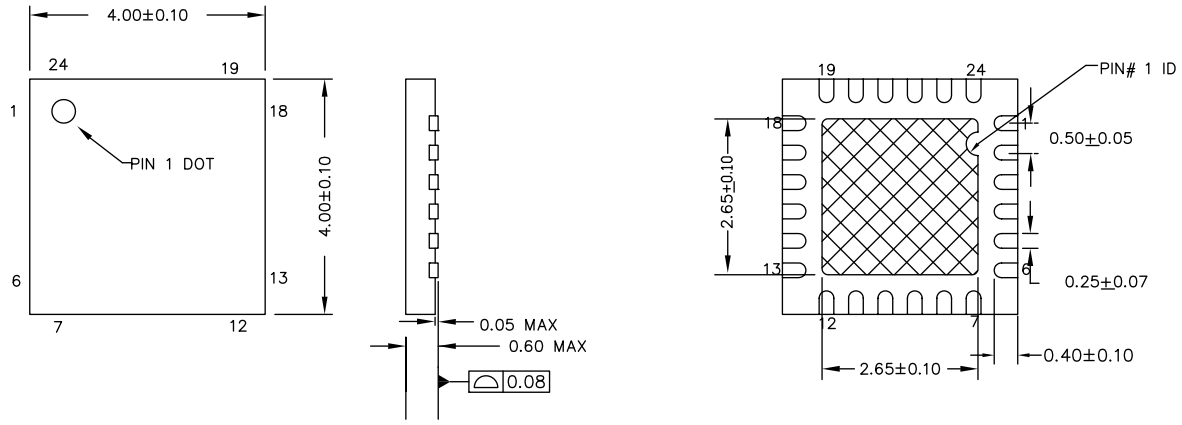
Cypress provides an extensive set of design guidelines for CapSense board designs. Refer to the CY8CMBR3xxx CapSense Design Guide for complete system guidelines.

The CY8CMBR3xxx family consists of six parts that vary depending on the parameters. The following table lists all the parts and a summary of the features supported. All package types are also available in Tape and Reel.

CY8CMBR3116-LQXI	24-pin QFN	Industrial	Up to 16	Up to 16	0	Up to 2	Up to 8	1	I^2C / GPO
CY8CMBR3106S-LQXI	24-pin QFN	Industrial	Up to 16	Up to 11	Up to 2	Up to 2	0	1	I^2C
CY8CMBR3110-SX2I	16-pin SOIC	Industrial	Up to 10	Up to 10	0	Up to 2	Up to 5	1	I^2C / GPO
CY8CMBR3108-LQXI	16-pin QFN	Industrial	Up to 8	Up to 8	0	Up to 2	Up to 4 + $\overline{HI}$	1	I^2C / GPO
CY8CMBR3102-SX1I	8-pin SOIC	Industrial	Up to 2	Up to 2	0	Up to 2	Up to 1	1	I^2C/GPO
CY8CMBR3002-SX1I	8-pin SOIC	Industrial	2	2	0	0	2	0	GPO



TOP VIEW SIDE VIEW BOTTOM VIEW

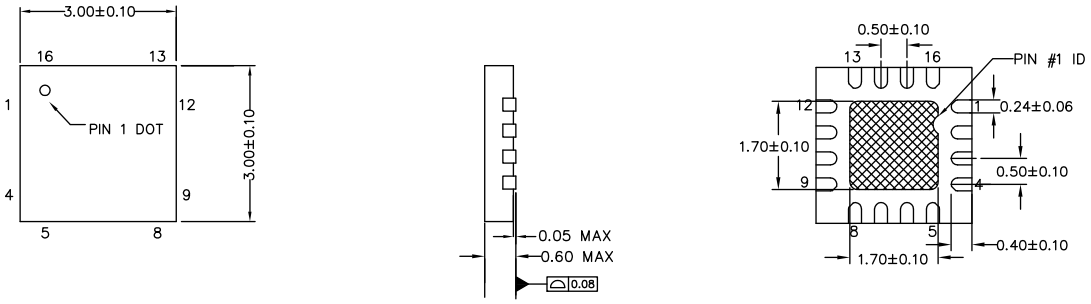


NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

TOP VIEW SIDE VIEW BOTTOM VIEW



NOTES

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web

001-87187 *A

T_A	Operating ambient temperature		–40	25	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (24-pin QFN)		–	38	–	°C/Watt
T_{JC}	Package θ_{JC} (24-pin QFN)		–	5.6	–	°C/Watt
T_{JA}	Package θ_{JA} (16-pin QFN)		–	49.6	–	°C/Watt
T_{JC}	Package θ_{JC} (16-pin QFN)		–	5.9	–	°C/Watt
T_{JA}	Package θ_{JA} (16-pin SOIC)		–	142	–	°C/Watt
T_{JC}	Package θ_{JC} (16-pin SOIC)		–	49.8	–	°C/Watt
T_{JA}	Package θ_{JA} (8-pin SOIC)		–	198	–	°C/Watt
T_{JC}	Package θ_{JC} (8-pin SOIC)		–	56.9	–	°C/Watt

Table 23 illustrates the minimum solder reflow peak temperature to achieve good solderability.

8-pin SOIC	260 °C	30 s
16-pin SOIC	260 °C	30 s
16-pin QFN	260 °C	30 s
24-pin QFN	260 °C	30 s

°C	degrees Celsius
fF	femtofarad
Hz	hertz
kbps	kilobits per second
kHz	kilohertz
kΩ	kilo ohm
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pp	peak-to-peak
pF	picofarad
s	second
V	volt

	Parasitic capacitance.
	The customizer tool (GUI) that enables easy register configurability and debugging for the CY8CMBR3xxx family of controllers.
	General Purpose Output – that is, an output pin on a chip that the user can configure.
	Flanking Sensor Suppression. An algorithm that distinguishes between signals from closely spaced buttons, eliminating false touches. It ensures that the system recognizes only the first button touched.
	Cypress CapSense algorithm that continuously compensates for system, manufacturing, and environmental changes.
	A ratio of the sensor signal, when touched, to the noise signal of an untouched sensor.
	An MBR device feature that toggles the state of GPOs on every sensor activation.
	An output pin drive mode wherein logic 0 is represented by a low voltage (that is, Voltage < V_{OL}), whereas logic 1 is represented by floating the output line to a HIGH impedance state.
	An output pin drive mode where logic 0 is represented by a low voltage (that is, Voltage < V_{OL}), whereas logic 1 is represented by a high voltage (that is, Voltage V > V_{OH}).
	A count value representing a digital count equivalent of sensed capacitance.
	A filtered version of the raw counts. The baseline essentially tracks the value of the parasitic capacitance in the system but does not track the value of the finger capacitance.
	The intrinsic capacitance of PC board traces to sensors.
	Additional capacitance introduced on a CapSense sensor when a finger approaches/touches the sensor.
	A setting value that is common for all elements of a set.
	A signal that indicates the active state by logic 0 and the inactive state by logic 1 values.
	A signal that indicates the active state by logic 1 and the inactive state by logic 0 values.
	A state where the device does not perform any processing and hence consumes less power.

CapSense CY8CMBR3xxx Design Guide	Provides design guidance for using capacitive touch sensing (CapSense) functionality with the CY8CMBR3xxx family of CapSense controllers.
Getting Started with CapSense®	Provides a starting point for anyone who is new to capacitive touch sensing (CapSense) and for anyone learning key design considerations and layout best practices.
Design Toolbox	Includes four sections – General Layout Guidelines for a CapSense PCB, a layout estimator for estimating button dimensions, a power consumption calculator (based on button dimensions), and the Design Validation tool to validate the layout design.
EZ-Click User Guide	Gives instructions on how to install and uninstall the EZ-Click Customizer tool and describes how to set up the boards. It also includes detailed descriptions of all the tabs in the GUI.
CY8CMBR3xxx Programming Specifications	Gives the information necessary to program the nonvolatile memory of the CY8CMBR3xxx devices. It describes the communication protocol required for access by an external programmer, explains the programming algorithm, and gives electrical specifications of the physical connection.
CapSense® Express™ Controllers Registers TRM	Lists and details all registers of CY8CMBR3102, CY8CMBR3106S, CY8CMBR3108, CY8CMBR3110, and CY8CMBR3116 CapSense® Express™ controllers. All registers are listed in the order of address.

*G	4359354	DCHE	05/06/2014	Updated links to the following web pages: EZ-Click, Cypress online store, and MBR3 Evaluation Kit. Changed time at max temperature from 20 seconds to 30 seconds.
*H	4557306	PRIA	11/26/2014	Replaced the term “water tolerance” with “liquid tolerance” wherever applicable. Added MPN versus Features Summary table. Corrected pin naming in the CY8CMBR3116 pin diagram (see Table 1). Added footnotes 2, 4, 6, 7, and 8 to specify AXRES pins. Changed “if unused” recommendation for I^2C lines to “pull-up” in the Pinouts section. Added details for Automatic Threshold feature. Mentioned about filters in Noise Immunity feature details. Added note to System Diagnostics feature ‘Sensor shorts’ to mention that sensor shorts can be detected for all pins other than AXRES. Added Register Configurability section. Mentioned that devices optimize power only when the I^2C bus is free in Power Consumption and Operational States. Updated I2C Communication Guidelines to mention that the devices also NACK to the first transaction in the Active state. Updated Figure 23 for clarity. Changed pin size “0.18–0.30” to “0.24 ± 0.06" Added definition of “low-power state” to Glossary.
*I	4626833	PRIA	01/16/2015	Added More Information. Moved CY8CMBR3xxx Ecosystem section to page 2.
*J	4681058	YLIU / PRIA	03/10/2015	Updated Ordering Information: Added Note “All package types are available in Tape and Reel.” and referred the same note in Table 21. Added Ordering Code Definitions.
*K	4735762	WKA	05/07/2015	Updated Packaging Dimensions: spec 001-13937 – Changed revision from *E to *F. Updated Thermal Impedances: Updated Table 22: Updated entire table.
*L	4812567	PRIA	06/26/2015	Updated MPN versus Features Summary: Updated details in “CY8CMBR3002” column corresponding to “Sensor auto-reset” feature. Updated details in “CY8CMBR3108” column corresponding to “Maximum number of GPOs/LED drive outputs” feature. Updated Pinouts: Recommended “If unused” connection for SPO, GPO and AXRES pins. Added Unused SPO Pin Connection. Added Unused SPO Pin Connection for AXRES pins. Added Unused GPO Pin Connection. Updated Power Consumption and Operational States: Removed low power design guidelines from this section, and referred to CY8CMBR3xxx Design Guide for these guidelines. Updated I2C Slave Address: Mentioned default I2C slave address for CY8CMBR3xxx devices. Provided details on how to configure the 7-bit I2C slave address for CY8CMBR3xxx devices.

(continued)

*M	5041506	PRIA	01/13/2016	Updated Power Supply Information: Updated description. Updated Power Consumption and Operational States: Updated description. Updated Figure 17. Updated Ordering Information: Removed the Note “All package types are available in Tape and Reel.” and its reference in Table 21, rather mentioned the same in description above Table 21. No change in part numbers. Updated Ordering Code Definitions (Added (T) and its details). Updated Packaging Dimensions: Updated “8-pin SOIC (150 Mils) Package Outline” to match latest packaging spec 51-85066 Rev *H. Updated to new template.

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