3.75kVrms/5.0kVrms Isolated Single Channel Gate Driver

Data Sheet

Pai821xx

FEATURES

Feature Options

- **Split Outputs Pai821x(A;B)**
- **Miller Clamp Pai821xC**

6A peak source and sink drive current

2.5V to 5.5V Input supply voltage

Up to 33V Driver supply voltage

8V and 12V UVLO options

3.75kVrms and 5.0kVrms isolation voltage

150kV/us typical CMTI

51ns typical propagation delay

CMOS inputs

Safety and regulatory approvals：

UL certificate number: E494497/(Pending)

3.75kVrms/5.0kVrms for 1 minute per UL 1577

VDE certificate number: 40052896/(Pending)

DIN VDE V 0884-11:2017-01

V_{IORM} = 1200V peak

CQC certification per GB4943.1-2011

Operating temperature range: -40°C to 125°C

RoHS-compliant, NB SOIC-8 and WB SOIC-8 package

APPLICATIONS

Switched-Mode Power Supplies

EV/HEV Inverters and DC/DC Converters

Solar Inverters

Motor Control

UPS and PSU

GENERAL DESCRIPTION

The Pai821xx is a single-channel isolated gate driver family with 3.75kVrms isolation voltage with NB SOIC-8 and 5.0kVrms isolation voltage with WB SOIC-8 per UL 1577. The Pai821x(A;B) provides a split output that controls the rise and fall times individually. The Pai821xC offers an internal clamp function connects the gate of the transistor to prevent false turn-on caused by miller current.

The Pai821xx output VCC operates range from 9.5V to 33V enables effective driving with Si or SiC MOSFET and IGBT power switches. Integrated UVLO protection ensures output held at low under abnormal conditions. The input VCC operates from 2.5V to 5.5V, which supports most digital controllers.

Compared to an optocoupler, Pai821xx has lower propagation delay, lower part-to-part skew, higher operating temperature and higher CMTI. It is very convenient to control MOSFET/IGBT gate drive across isolation barrier or with level shifting.

Device Information

PART SERIES	UVLO	PIN CONFIGURATION
Pai821xA	8V	Split output
Pai821xB	12V	Split output
Pai821xC	12V	Miller clamp

FUNCTIONAL BLOCK DIAGRAMS

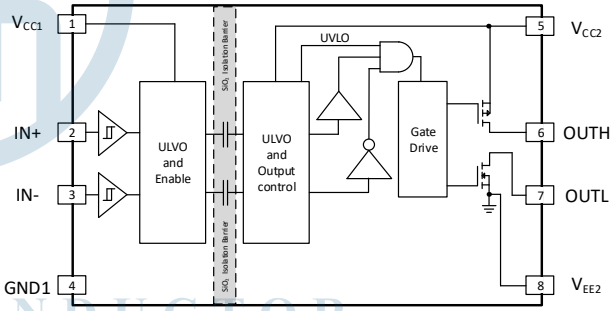


Figure1. Pai821x(A;B) Functional Block Diagrams

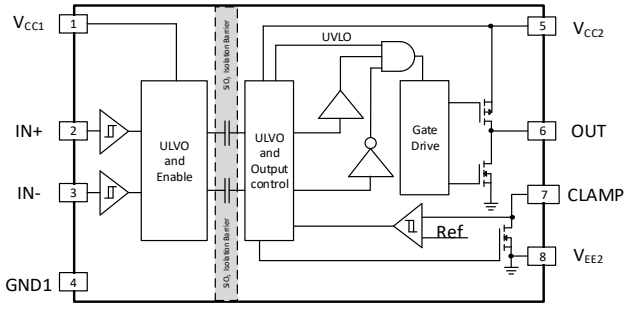


Figure2. Pai821xC Functional Block Diagrams

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Room 307-309, No.22, Boxia Road, Pudong New District, Shanghai, 201203, China
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PIN CONFIGURATIONS AND FUNCTIONS

Table1. Pai821x(A;B) Pin Function Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	V_{CC1}	P	Input Power Supply
2	IN+	I	Positive Input
3	IN-	I	Negative Input
4	GND1	G	Input Ground
5	V_{CC2}	P	Output Power Supply
6	OUTH	O	Pull High Output
7	OUTL	O	Pull Low Output
8	V_{EE2}	G	Output Ground

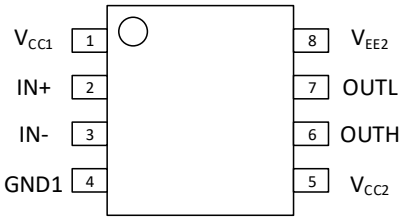


Figure3. Pai821x(A;B) Pin Configuration

Table2. Pai821xC Pin Function Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	V_{CC1}	P	Input Power Supply
2	IN+	I	Positive Input
3	IN-	I	Negative Input
4	GND1	G	Input Ground
5	V_{CC2}	P	Output Power Supply
6	OUT	O	Gate-Drive Output
7	CLAMP	O	Active Miller Clamp
8	V_{EE2}	G	Output Ground

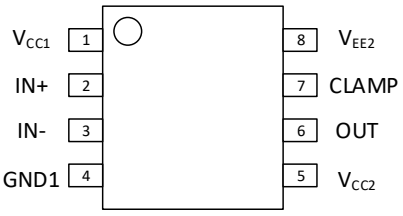


Figure4. Pai821xC Pin Configuration

SPECIFICATIONS

Absolute Maximum Ratings

Table3. Pai821xx Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

DESCRIPTION		MIN	MAX	UNIT
V_{CC1}	Input supply voltage (reference to GND1)	-0.3	7	V
V_{In+}, V_{In-}	Signal input voltage	-0.3	V_{CC1}+0.3	V
V_{CC2}	Output supply voltage (reference to V_{EE2})	-0.3	36	V
Output signal voltage	V_{OUTH}-V_{EE2}, V_{OUTL}-V_{EE2}, V_{OUT}-V_{EE2}, V_{CLAMP}-V_{EE2}	V_{EE2}-0.3	V_{CC2}+0.3	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

ESD Rating

Table4. Pai821xx ESD Ratings

DESCRIPTION		Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-6000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-2000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Table5. Pai821xx Recommended Operating Conditions

DESCRIPTION		MIN	MAX	UNIT
V_{CC1}, V_{In+}, V_{In-}	Input supply voltage and input side signal voltage	2.5	5.5	V
V_{CC2}	Output supply voltage for Pai821xA	9.5	33	V
V_{CC2}	Output supply voltage for Pai821x(B;C)	13.2	33	V
T_A	Ambient temperature	-40	125	°C

Truth Table

Table6. Pai821x(A;B) Truth Table

V_{CC1}	IN+	IN-	V_{CC2}	OUTH	OUTL
above UVLO	L(1) or floating	X	above UVLO	Hi-Z	L
above UVLO	H	H or floating	above UVLO	Hi-Z	L
above UVLO	H	L	above UVLO	H	Hi-Z
X	X	X	below UVLO	Hi-Z	L
below UVLO	X	X	X	Hi-Z	L

(1) L=Logic Low, H= Logic High, X=H, L or floating, Hi-Z= High impedance.

Table7. Pai821xC Truth Table

V_{CC1}	IN+	IN-	V_{CC2}	OUT	CLAMP
above UVLO	L(1) or floating	X	above UVLO	L	L
above UVLO	H	H or floating	above UVLO	L	L
above UVLO	H	L	above UVLO	H	Hi-Z
X	X	X	below UVLO	L	L
below UVLO	X	X	X	L	L

(1) L=Logic Low, H= Logic High, X=H, L or floating, Hi-Z= High impedance.

Thermal Information

Table8. Pai821xx Thermal Information

PACKAGE THERMAL RATINGS	NB SOIC-8	WB SOIC-8	UNIT
$R_{\theta JA}$ Junction-to-Ambient thermal resistance	110	110	°C/W
Ψ_{JT} Junction–to-top characterization parameter	18	18	°C/W

Supply Power Ratings

Table9. Pai821xx-SR NB SOIC-8 Package Supply Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D Maximum power dissipation on input and output	V_{CC1} = 5 V, V_{CC2} = 15 V, f = 1.8MHz,50% duty cycle, square wave, 2.2nF load			1.14	W
P_{D1} Maximum input power dissipation				0.01	W
P_{D2} Maximum output power dissipation				1.13	W

Table10. Pai821xx-W5R WB SOIC-8 Package Supply Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D Maximum power dissipation on input and output	V_{CC1} = 5 V, V_{CC2} = 15 V, f = 1.8MHz,50% duty cycle, square wave, 2.2nF load			1.14	W
P_{D1} Maximum input power dissipation				0.01	W
P_{D2} Maximum output power dissipation				1.13	W

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Electrical Specifications

Table11. Pai821xx Electrical Specifications

V_{CC1} = 2.5V_{DC} or 3.3V_{DC} or 5V_{DC}, 0.1uF capacitor from V_{CC1} to GND1, V_{CC2} = 15V_{DC}, 1uF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} =1nF. T_A = –40°C to 125°C (Unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS					
I_{VCC1} V_{CC1} quiescent current	V_{IN-}=0V, V_{IN+}=0V		0.8	1.2	mA
I_{VCC2} V_{CC2} quiescent current	V_{IN-}=0V, V_{IN+}=0V		1.8	2.7	mA
SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS					
$V_{UV+(VCC1)}$	V_{VCC1} Undervoltage Rising Threshold	2.10	2.25	2.40	V
$V_{UV-(VCC1)}$	V_{VCC1} Undervoltage Falling Threshold	2.00	2.10	2.20	V
$V_{HYS(VCC1)}$	V_{VCC1} UVLO threshold hysteresis	0.10	0.15		V
Pai821XA DRIVER SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS					
$V_{UV+(VCC2)}$	V_{VCC2} Undervoltage Rising Threshold		8.4	9.4	V
$V_{UV-(VCC2)}$	V_{VCC2} Undervoltage Falling Threshold	7.1	7.8		V
$V_{HYS(VCC2)}$	V_{VCC2} UVLO threshold hysteresis		0.6		V

Pai821X(B:C) DRIVER SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS					
$V_{UV+(VCC2)}$	V_{VCC2} Undervoltage Rising Threshold		12	13	V
$V_{UV-(VCC2)}$	V_{VCC2} Undervoltage Falling Threshold	9.8	10.8		V
$V_{HYS(VCC2)}$	V_{VCC2} UVLO threshold hysteresis		1.2		V
INPUT					
V_{INH} Input rising threshold			0.50*V_{CC1}	0.60*V_{CC1}	V
V_{INL} Input falling threshold		0.30*V_{CC1}	0.35*V_{CC1}		V
V_{HYS}			0.15*V_{CC1}		
OUTPUTS					
I_{OH}/I_{OL} Peak source and sink current	C_{LOAD} = 0.22uF, with external current limiting resistors, 1kHz switching frequency	6	10		A
V_{OH} High-level output voltage (V_{CC2}-V_{OUTH})	I_{OUTH}= –20 mA		100	150	mV
V_{OL} Low level output voltage (V_{OUTH}-V_{OUTL})	I_{OUTL} = 20mA		7.5	11.5	mV
ACTIVE MILLER CLAMP (Pai821XC only)					
V_{CLAMP} Low level clamp voltage	I_{CLAMP} = 20 mA		7	10	mV
I_{CLAMP} Clamp low level current	V_{CLAMP} = V_{EE2} + 15 V		10		A
$V_{CLAMP-TH}$ Clamp threshold voltage	IN+=high, IN-=low		2.1	2.3	V
SHORT CIRCUIT CLAMPING (Pai821XC only)					
$V_{CLP-OUT}$ Clamping voltage (V_{OUT}-V_{CC2})	IN+=high, IN-=low, t_{CLAMP}=10us, I_{OUT}=500mA		1.0	1.3	V
$V_{CLP-OUT}$ Clamping voltage (V_{CC2}-V_{CLAMP})	IN+=low, IN-=high, I_{CLAMP}=-20mA		0.9	1.0	V
ACTIVE PULLDOWN (Pai821XC only)					
V_{OUTSD} Active pulldown voltage on CLAMP	I_{OUT}=0.1x$I_{OUTL(typ)}$, V_{CC2}=open		1.8	2.5	V
TIMING					
t_{PLH} Propagation delay, high[1] t_{PHL} Propagation delay, low[1]	C_{LOAD} = 1.8nF		51 51	65 65	ns
t_{PWD} Pulse Width Distortion	C_{LOAD} = 1.8nF		1	10	ns
t_r Rise time[2] t_f Fall time[2]	C_{LOAD} = 1.8nF		8 7	15 12	ns
CMTI	Common-mode transient immunity[3]		150		kV/us

(1) t_{PLH} = low-to-high propagation delay time, t_{PHL} = high-to-low propagation delay time. See Figure22.

(2) t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal，t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal. See Figure21.

(3) See Figure28 for Common-mode transient immunity (CMTI) measurement.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Insulation Specifications

Table12. Pai821xx Insulation Specifications

PARAMETER	SYMBOL	VALUE		UNIT	TEST CONDITIONS/COMMENTS
		NB SOIC-8	WB SOIC-8		
Rated Dielectric Insulation Voltage		3750	5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	⩾4	⩾8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	⩾4	⩾8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		⩾21	⩾21	μm	Insulation distance through insulation

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PARAMETER	SYMBOL	VALUE		UNIT	TEST CONDITIONS/COMMENTS
		NB SOIC-8	WB SOIC-8		
Tracking Resistance (Comparative Tracking Index)	CTI	>400	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II	II		Material Group (DIN VDE 0110, 1/89, Table 1)

Package Specifications

Table13. Pai821xx Package Specifications

PARAMETER	SYMBOL	TYPICAL VALUE	UNIT	TEST CONDITIONS/COMMENTS
Resistance (Input to Output)[1]	R_{I-O}	10^{11}	Ω	
Capacitance (Input to Output)[1]	C_{I-O}	1.5	pF	@1MHz
Input Capacitance[2]	C_I	3	pF	@1MHz

(1) The device is considered a 2-terminal device; SOIC-8 Pin 1 - Pin 4 are shorted together as the one terminal, and SOIC-8 Pin 5 - Pin 8 are shorted together as the other terminal.

(2) Testing from the input signal pin to ground.

Regulatory Information

Table14. Pai821xx Regulatory Information

The Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Regulatory	Pai821xx-SR (NB SOIC-8 Package)	Pai821xx-W5R (WB SOIC-8 Package)
UL	Recognized under UL 1577 Component Recognition Program1 Single Protection, 3750V rms Isolation Voltage File Number: **E494497**	Recognized under UL 1577 Component Recognition Program1 Single Protection, 5000V rms Isolation Voltage File (Pending)
VDE	DIN VDE V 0884-11:2017-012 Basic insulation, VIORM = 1200V peak, VIOSM = 5000 V peak File Number: **40052896**	DIN VDE V 0884-11:2017-012 Basic insulation, VIORM = 1200V peak, VIOSM = 5000 V peak File (Pending)
CQC	Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at 500 V rms (707 V peak) working voltage Reinforced insulation at 422 V rms (600 V peak) File Number: **CQC22001333773**	Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at 500 V rms (707 V peak) working voltage Reinforced insulation at 422 V rms (600 V peak) File (Pending)

(1) In accordance with UL 1577, each Pai821xx-SR is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec; each Pai821xx-W5R is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.

(2) In accordance with DIN V VDE V 0884-11, each Pai821xx is proof tested by applying an insulation test voltage ≥ 1800V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-11 approval.

VDE Insulation Characteristics

Table15. VDE Insulation Characteristics

DESCRIPTION	TEST CONDITIONS/COMMENTS	SYMBOL	CHARACTERISTIC		Unit
			Pai821xx-SR NB SOIC-8	Pai821xx-W5R WB SOIC-8	
Overvoltage Category per IEC 60664-1	For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms		I to IV I to III I to III	I to IV I to III I to III	
Climatic Classification			40/105/21	40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	

DESCRIPTION	TEST CONDITIONS/COMMENTS	SYMBOL	CHARACTERISTIC		Unit
			Pai821xx-SR NB SOIC-8	Pai821xx-W5R WB SOIC-8	
Maximum repetitive peak isolation voltage		V_{IORM}	1200	1200	V peak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.5 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1800	1800	V peak
Input to Output Test Voltage, Method A		$V_{pd(m)}$			
After Environmental Tests Subgroup 1	V_{IORM} × 1.2 = $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1440	1440	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1440	1440	V peak
Highest Allowable Overvoltage		V_{IOTM}	5300	7071	V peak
Surge Isolation Voltage Basic	Basic insulation, 1.2/50 µs combination wave, VTEST = 1.3 × VIOSM (qualification)[1]	V_{IOSM}	5000	5000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure6)				
Maximum safety Temperature		T_S	150	150	°C
Maximum Power Dissipation at 25°C		P_S	1.14	1.14	W
Insulation Resistance	V_{IO} = 500 V at T_A=25°C	R_{IO}	$>10^{12}$	$>10^{12}$	Ω
	V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
	V_{IO} = 500 V at T_S=150°C	R_{IO}	$>10^{9}$	$>10^{9}$	Ω

(1) In accordance with DIN V VDE V 0884-11, Pai821xx is proof tested by applying a surge isolation voltage 6500V.

TYPICAL CHARACTERISTIC

V_{CC1}=2.5V_{DC} or 3.3V_{DC} or 5V_{DC}, 0.1uF capacitor from V_{CC1} to GND1, V_{CC2} = 15V_{DC}, 1uF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} =1nF. T_A = –40°C to 125°C (Unless otherwise noted).

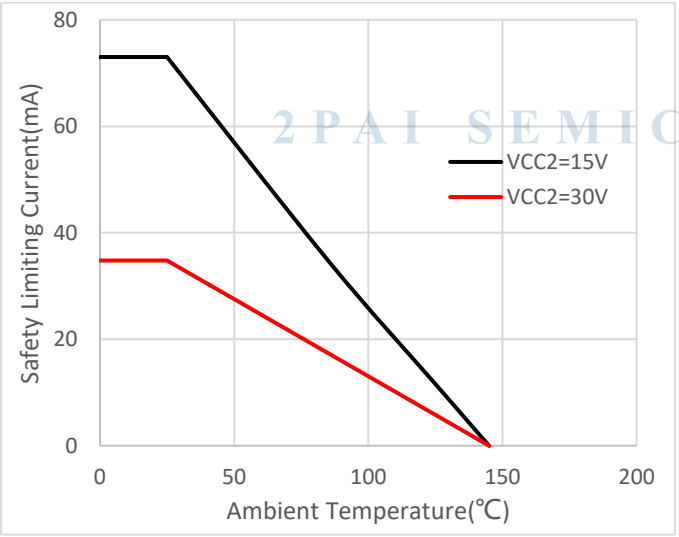


Figure5. NB/WB SOIC-8 Thermal Derating Curve for Limiting Current with Ambient Temperature per VDE

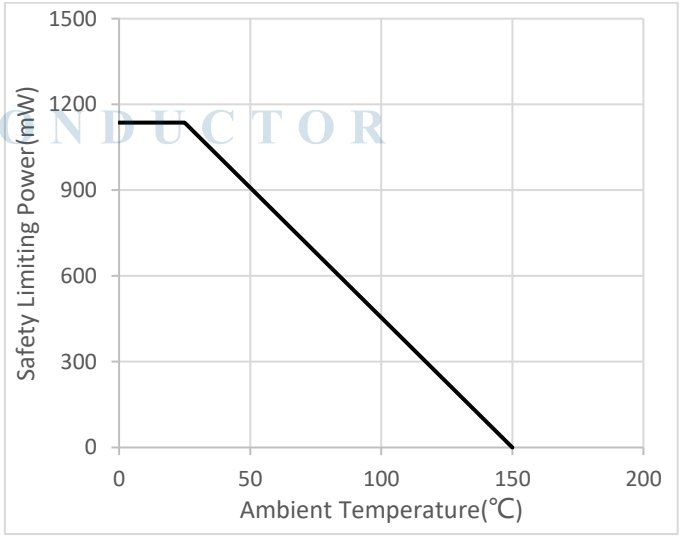


Figure6. NB/WB SOIC-8 Thermal Derating Curve for Limiting Power with Ambient Temperature per VDE

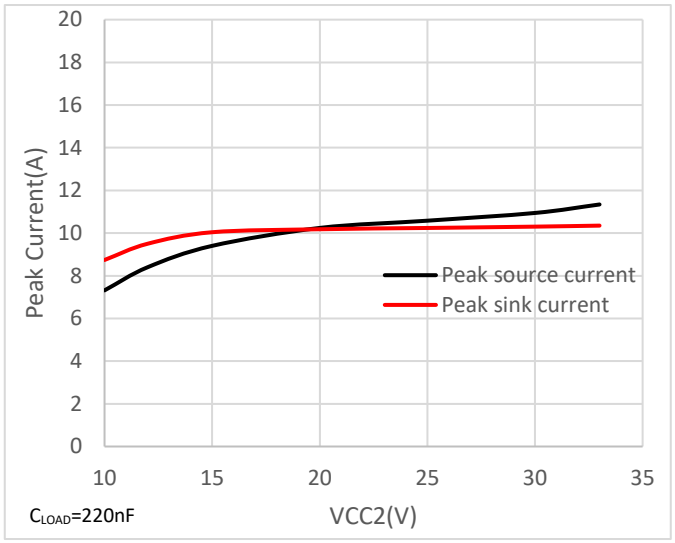


Figure7. Output High Drive Current vs V_{CC2}

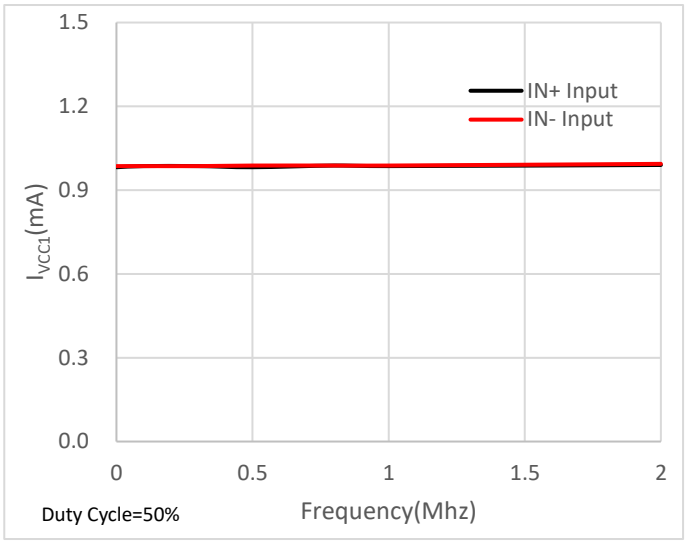


Figure8. I_{VCC1} Supply Current vs Input Frequency

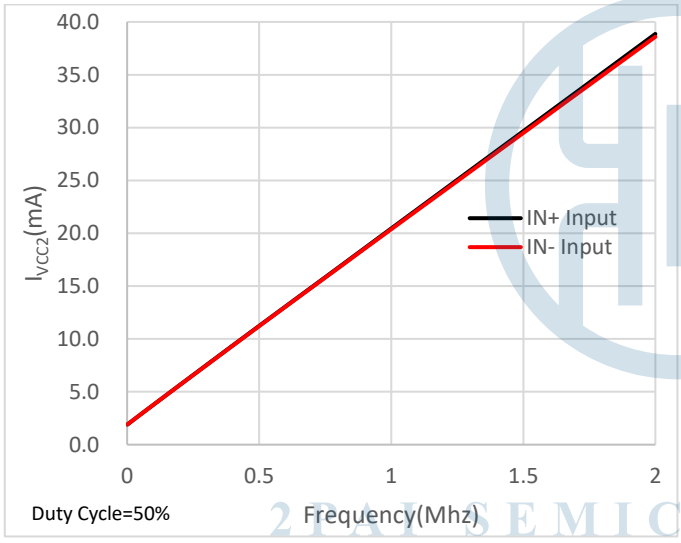


Figure9. I_{VCC2} Supply Current vs Input Frequency

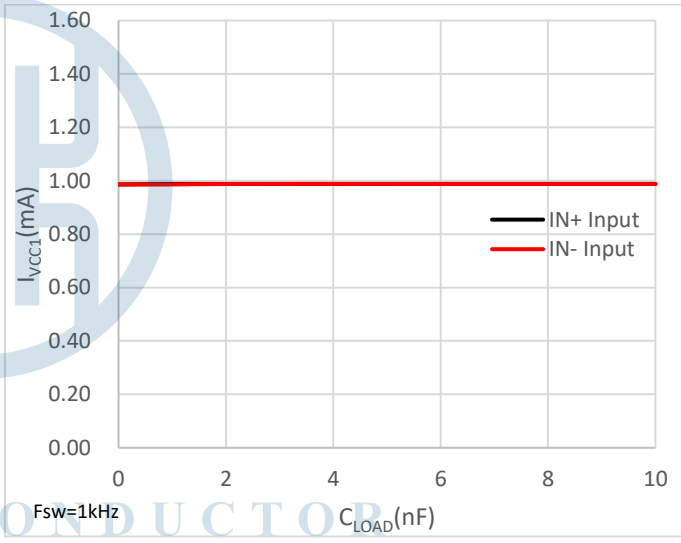


Figure10. I_{VCC1} Supply Current vs Load Capacitance

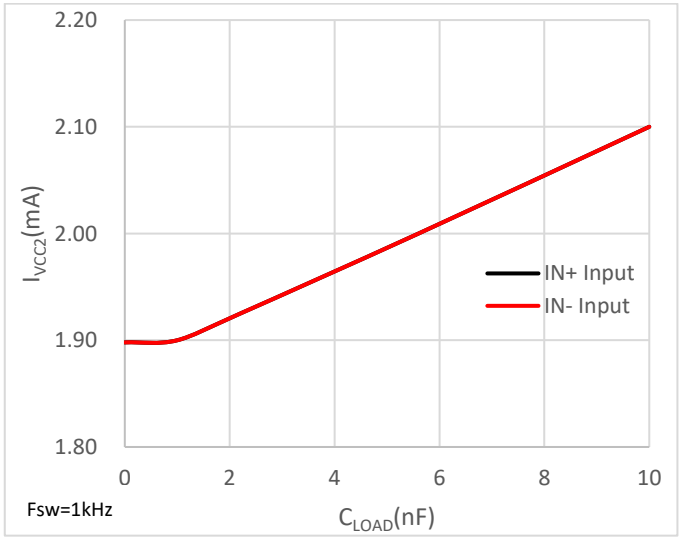


Figure11. I_{VCC2} Supply Current vs Load Capacitance

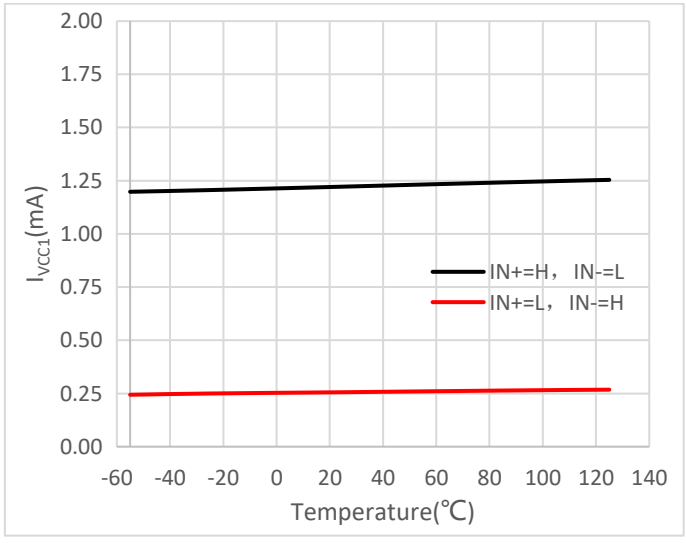


Figure12. I_{VCC1} Supply Current vs Ambient Temperature

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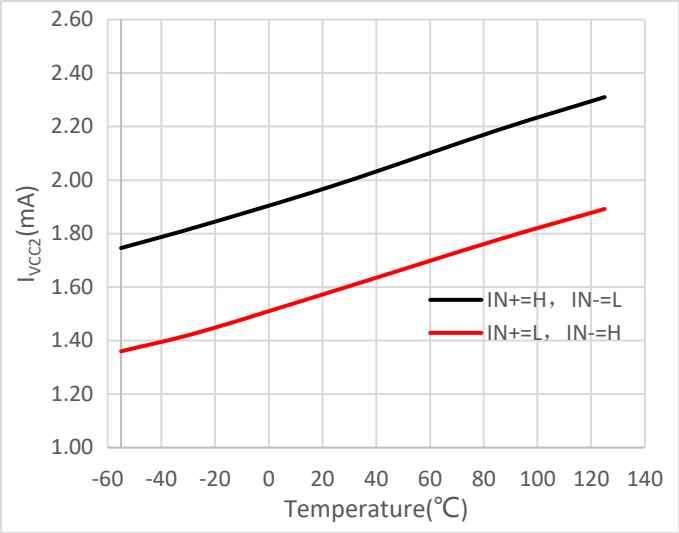


Figure13. I_{VCC2} Supply Current vs Ambient Temperature

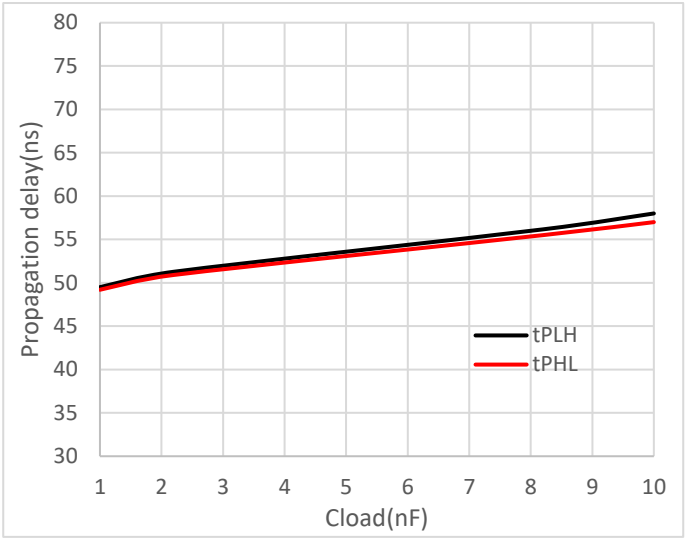


Figure14. Propagation Delay vs Load Capacitance

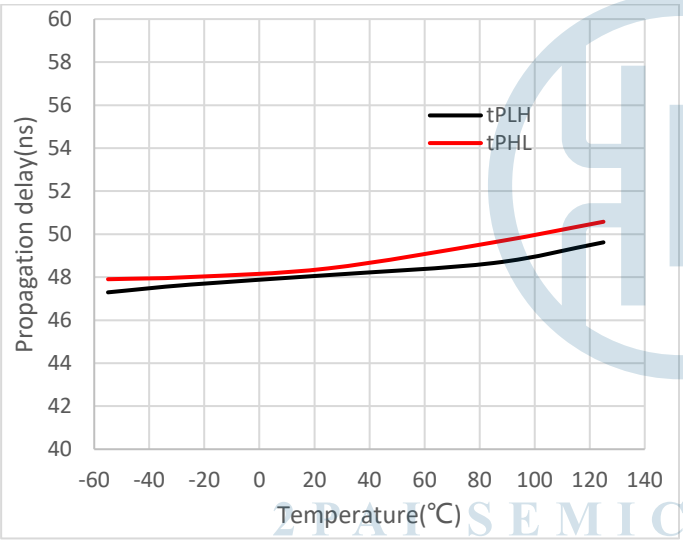


Figure15. Propagation Delay vs Ambient Temperature

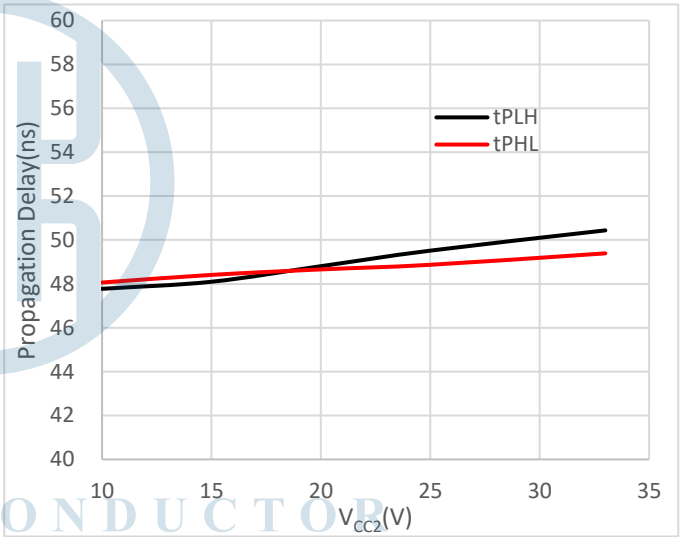


Figure16. Propagation Delay vs V_{CC2}

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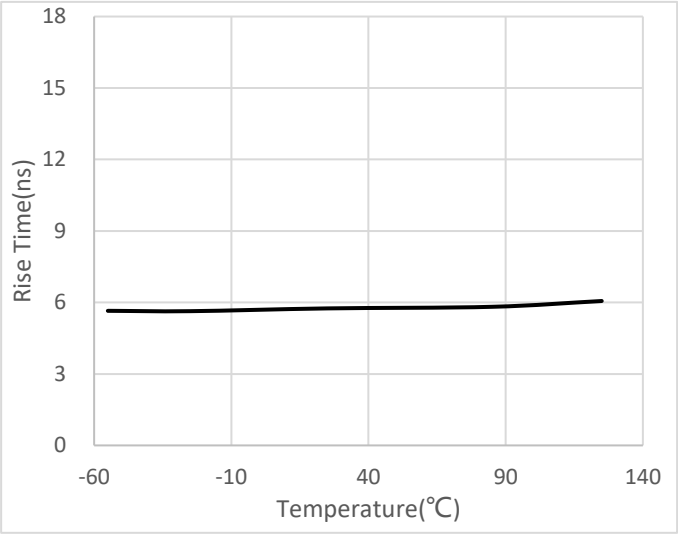


Figure17. Rise Time vs Ambient Temperature

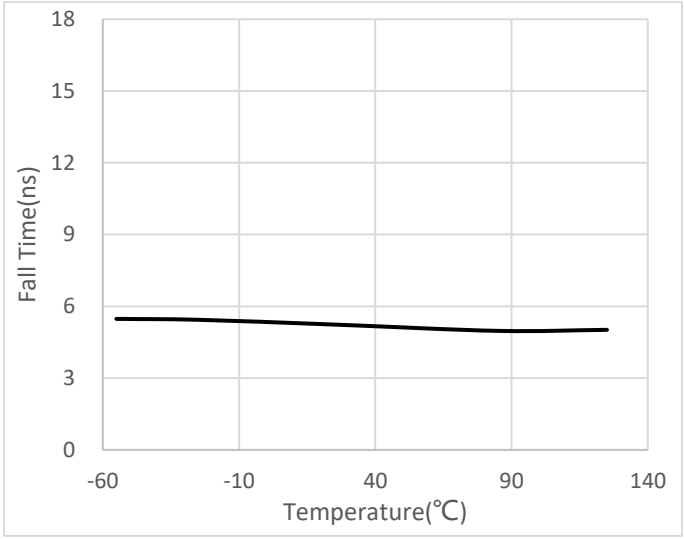


Figure18. Fall Time vs Ambient Temperature

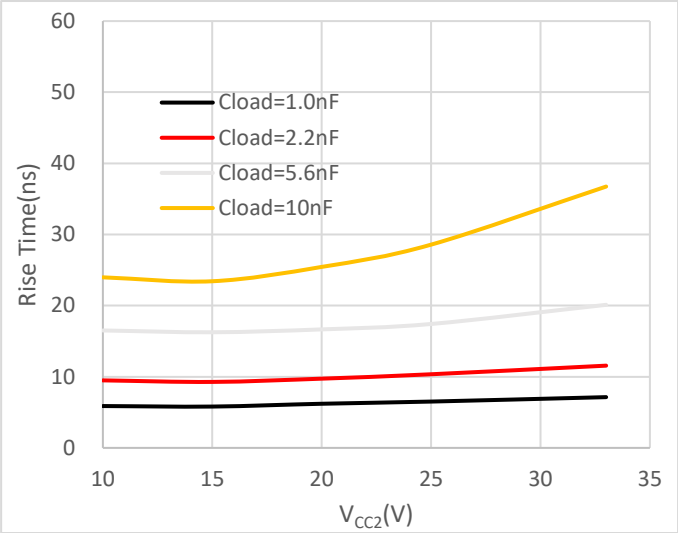


Figure19. Rise Time vs C_{LOAD} and V_{CC2}

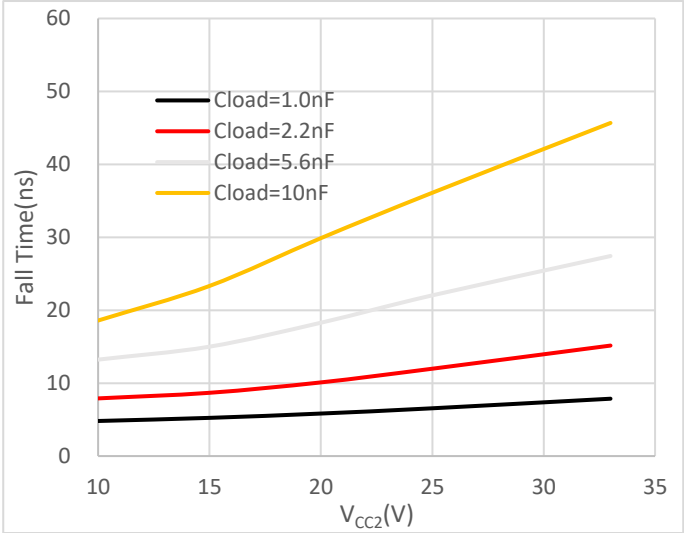


Figure20. Fall Time vs C_{LOAD} and V_{CC2}

TIMING TEST INFORMATION

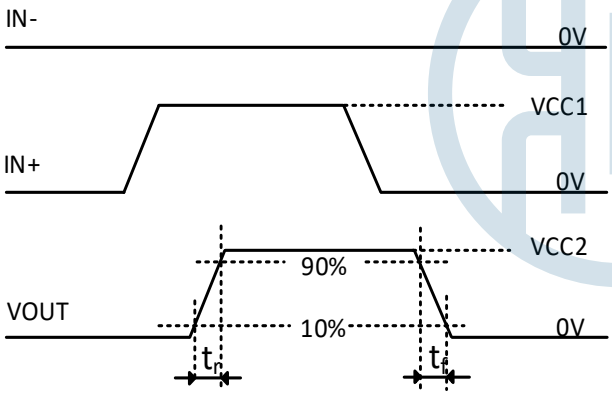


Figure21. Transition time waveform measurement

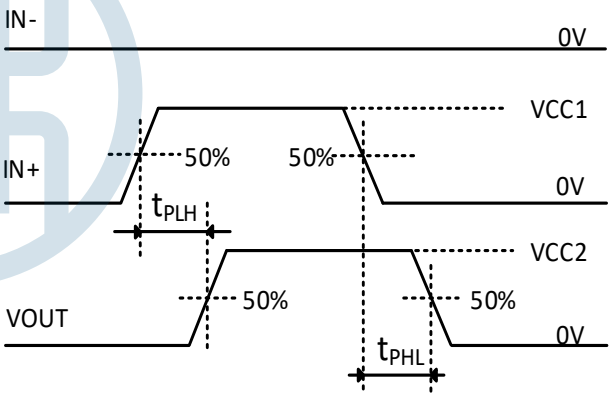


Figure22. Propagation delay time waveform measurement

2PAI SEMICONDUCTOR

APPLICATIONS INFORMATION

Typical Application

The circuit figure below is a typical application for driving IGBTS.

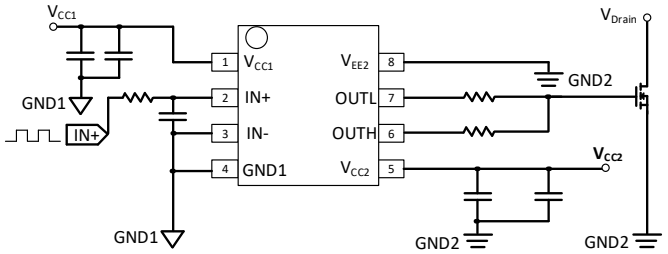


Figure23. Pai821x(A;B) typical application circuit (IN+ Input)

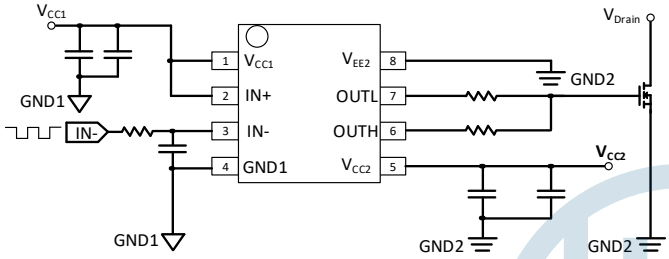


Figure24. Pai821x(A;B) typical application circuit (IN- Input)

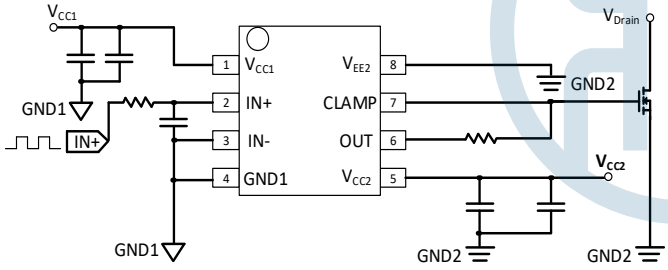


Figure25. Pai821xC typical application circuit (IN+ Input)

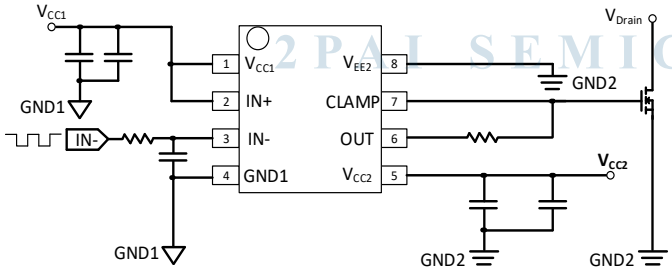


Figure26. Pai821xC typical application circuit (IN- Input)

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{CC1} and GND1 and between V_{CC2} and V_{EE2}. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value between V_{CC1} and GND1 is between 0.1 µF and 1µF, bypass capacitor value between V_{CC2} and V_{EE2} is between 1 µF and 10 µF. Additional 100nF capacitor in parallel with the isolator device bypass capacitor is recommended for high frequency filtering.

To avoid large negative transients on the VEE2 pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

Avoid reducing the isolation capability, keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

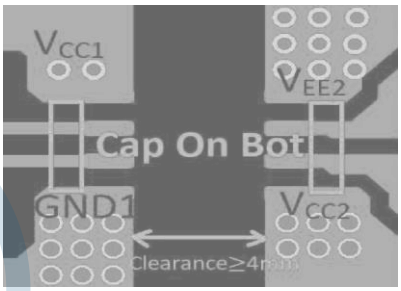


Figure27. Layout example

MILLER CLAMP (Pai821XC only)

The active Miller-clamp function is used to prevent false turn-on of the power switches caused by Miller current with applications where a unipolar power supply is used. Low impedance path between the power-switch gate terminal and Miller clamp pins to sink the Miller current is available for the active Miller-clamp function implemented. Witch the Miller-clamp function, the power-switch gate voltage is clamped to less than 2V during the off state.

The Pai821xC provides short-circuit clamping function to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the VCC2 voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the VCC2 pin inside the driver. The internal diodes can conduct up to 500mA current for a duration of 10µs and a continuous current of 20mA. Use external Schottky diodes to improve current conduction capability as needed.

The active pulldown function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the VCC2 supply. This feature prevents IGBT and MOSFET false turn-on on the OUT and CLAMP pins by clamping the output voltage to approximately 2 V.

Figure25 and Figure26 shows a typical application circuit of Pai821xC.

2PAI SEMICONDUCTOR

CMTI MEASUREMENT

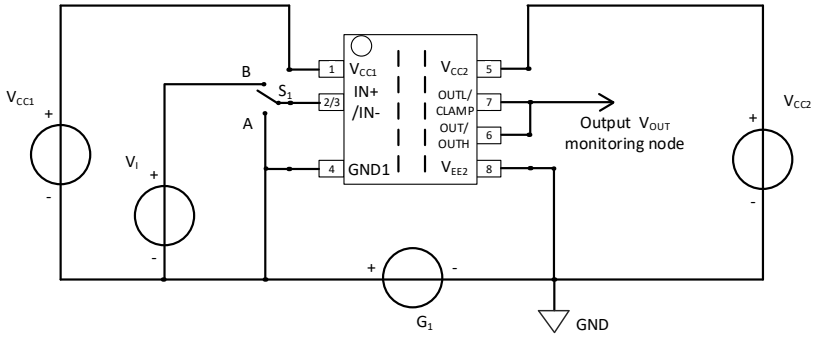
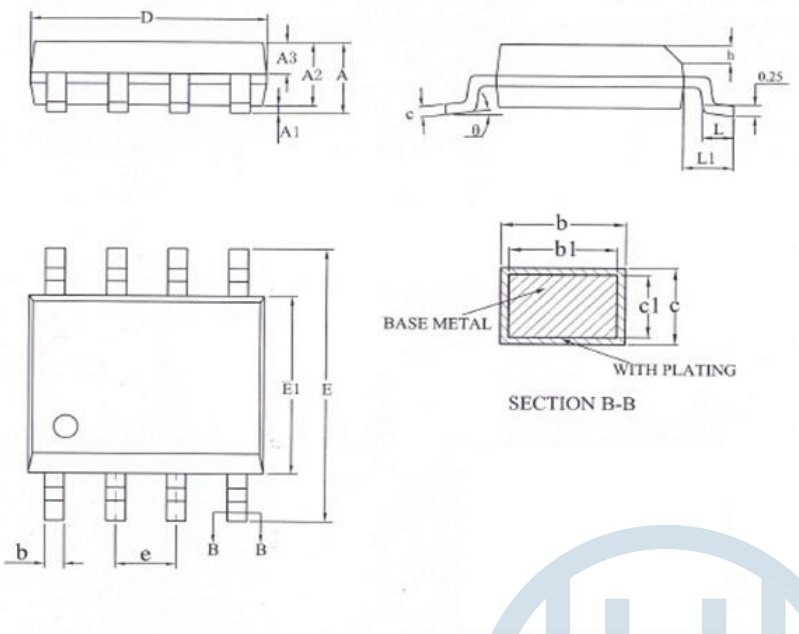


Figure28. Common-mode transient immunity (CMTI) measurement

To measure the Common-Mode Transient Immunity (CMTI) of Pai821xxx isolated gate driver under specified common-mode pulse magnitude (VCM) and specified slew rate of the common-mode pulse (dVCM/dt) and other specified test or ambient conditions, The common-mode pulse generator (G1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (VCM),such that the maximum common-mode slew rates (dVCM/dt) can be applied to Pai821xxx isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground V_{EE2} of Pai821xxx isolated gate driver, with positive transients as well as negative transients.

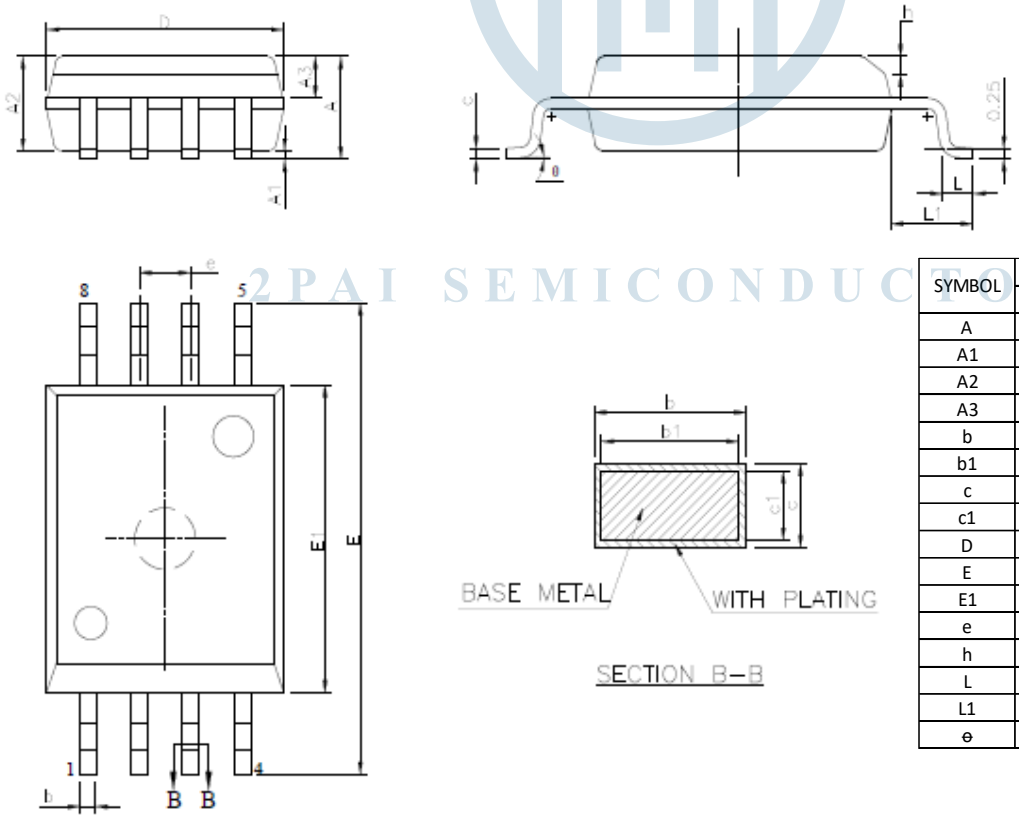
2PAI SEMICONDUCTOR

OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

Figure29. 8-Lead Narrow Body SOIC [NB SOIC-8] *Outline Package–dimension unit(mm)*



2PAI SEMICONDUCTOR

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	1.00
L1	2.00REF		
θ	0	-	8°

Figure30. 8-Lead Wide Body SOIC [WB SOIC-8] *Outline Package–dimension unit(mm)*

LAND PATTERNS

8-Lead Narrow Body SOIC [NB SOIC-8]

The figure below illustrates the recommended land pattern details for the Pai82xxxx in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

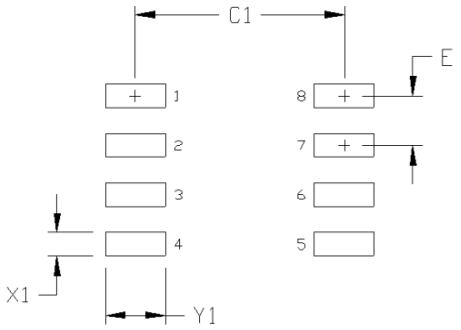


Figure31. 8-Lead Narrow Body SOIC [NB SOIC-8] Land Pattern

Table16. NB SOIC-8 Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	5.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.55	mm

(1) This land pattern design is based on IPC -7351.
(2) All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

8-Lead Wide Body SOIC [WB SOIC-8]

The figure below illustrates the recommended land pattern details for the Pai1xxxxx in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

2PAI SEMICONDUCTOR

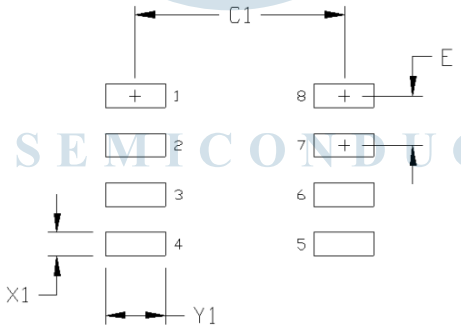


Figure32. 8-Lead Wide Body SOIC [WB SOIC-8] Land Pattern

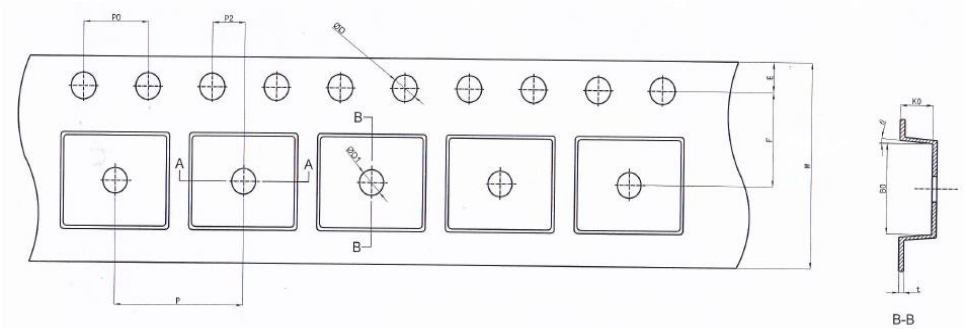
Table17.8-Lead Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	9.75	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	2.00	mm

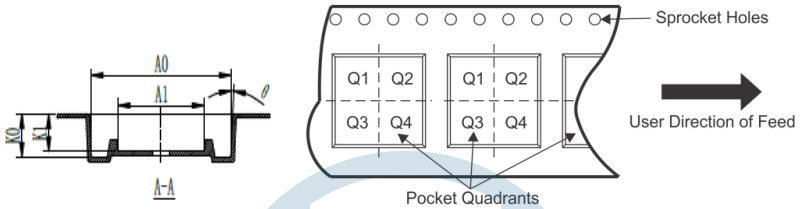
(1) This land pattern design is based on IPC -7351.
(2) All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

REEL INFORMATION

8-Lead Narrow Body SOIC [NB SOIC-8]



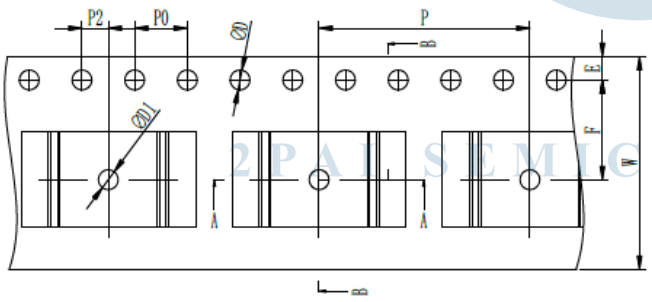
COMMON SIZE		POCKET SIZE	
APPEARANCE	DIMENSION(MM)	APPEARANCE	DIMENSION(MM)
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10	t	0.30±0.05
10P0	40.0±0.20	θ	3° TYP



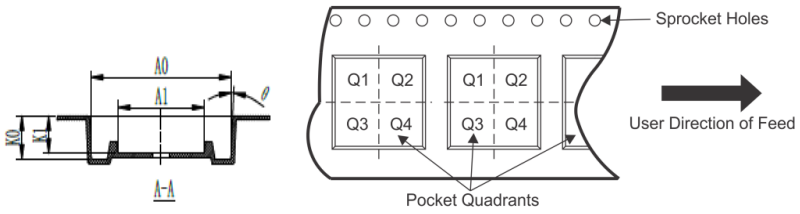
Note：The Pin 1 of the chip is in the quadrant Q1

Figure33. 8-Lead Narrow Body SOIC [NB SOIC-8] Reel Information–*dimension unit(mm)*

8-Lead Wide Body SOIC [WB SOIC-8]



COMMON SIZE		POCKET SIZE	
APPEARANCE	DIMENSION(MM)	APPEARANCE	DIMENSION(MM)
E	1.75±0.10	W	16.00±0.30
F	7.50±0.10	P	16.00±0.10
P2	2.00±0.10	A0	11.98±0.10
D	$1.50^{+0.1}_{0}$	A1	7.37±0.10
D1	$1.50^{+0.1}_{0}$	B0	6.11±0.10
P0	4.00±0.10	K0	3.00±0.10
10P0	40.0±0.20	K1	2.60±0.10
		t	0.3±0.05
		θ	5° TYP



Note：The Pin 1 of the chip is in the quadrant Q1

Figure34. 8-Lead Wide Body SOIC [WB SOIC-8] Reel Information–*dimension unit(mm)*

Top Marking



Line 1	Pai82XXX=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXXX, no special meaning

Figure 35. *Top Marking*

ORDERING GUIDE

Table18. Ordering Guide

Model Name	Temperature Range	UVLO (V)	Output Current (A)	Isolation Rating (kV rms)	AEC-Q100	Package	MSL Peak Temp [1]	MOQ/ Quantity per reel[2]
Pai8211A-SR	−40 to 125°C	8	6	3.75	NO	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211AQ-SR	−40 to 125°C	8	6	3.75	YES	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211B-SR	−40 to 125°C	12	6	3.75	NO	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211BQ-SR	−40 to 125°C	12	6	3.75	YES	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211C-SR	−40 to 125°C	12	6	3.75	NO	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211CQ-SR	−40 to 125°C	12	6	3.75	YES	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211A-W5R	−40 to 125°C	8	6	5.00	NO	WB SOIC-8	Level-2-260C-1 YEAR	1000
Pai8211AQ-W5R	−40 to 125°C	8	6	5.00	YES	WB SOIC-8	Level-2-260C-1 YEAR	1000
Pai8211B-W5R	−40 to 125°C	12	6	5.00	NO	WB SOIC-8	Level-2-260C-1 YEAR	1000
Pai8211BQ-W5R	−40 to 125°C	12	6	5.00	YES	WB SOIC-8	Level-2-260C-1 YEAR	1000
Pai8211C-W5R	−40 to 125°C	12	6	5.00	NO	WB SOIC-8	Level-2-260C-1 YEAR	1000
Pai8211CQ-W5R	−40 to 125°C	12	6	5.00	YES	WB SOIC-8	Level-2-260C-1 YEAR	1000

(1) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(2) MOQ, minimum ordering quantity.

RPAI SEMICONDUCTOR

REVISION HISTORY

Revision	Date	Page	Change Record
1.0	2021/08/12	All	Initial version
1.1	2022/07/20	All	Change Level 3 to level 2(Pending) Changed Regulatory Information Added Pai8211(B;C) and WB SOIC-8 package information.

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